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This patent is subject to a terminal disclaimer.

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Primary Examiner—Thanh Cong Le

Assistant Examiner—Thuan T. Nguyen

(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

A transmitter-receiver circuit for radio communication, comprising a low-noise receiver amplifier (20); a first matching circuit (40) which converts the input impedance of the amplifier (20); a transmitter amplifier (10) including a second matching circuit (50) and a third matching circuit (60) which convert the impedances to transmitting signals; and a mode switch (30) for changing from transmitting to receiving and vice versa. The transmitter amplifier (10) has a control terminal (14) connected to the gate electrode of a high-power FET (12), and the output terminal (15A) of the terminal (10) is connected to an antenna (80) not through the switch (30).

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- (52) **U.S. Cl.** **455/83; 455/78; 455/129**

- (58) **Field of Search** 455/78, 80, 82,
455/83, 84, 89, 90, 129; 333/101, 103,
104

4 Claims, 11 Drawing Sheets

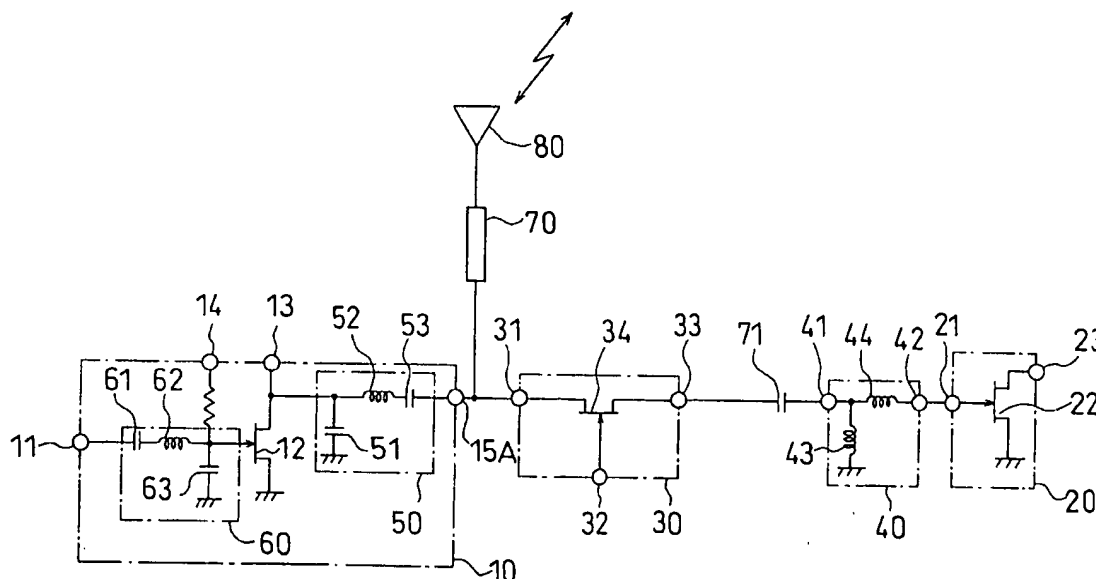


Fig. 1

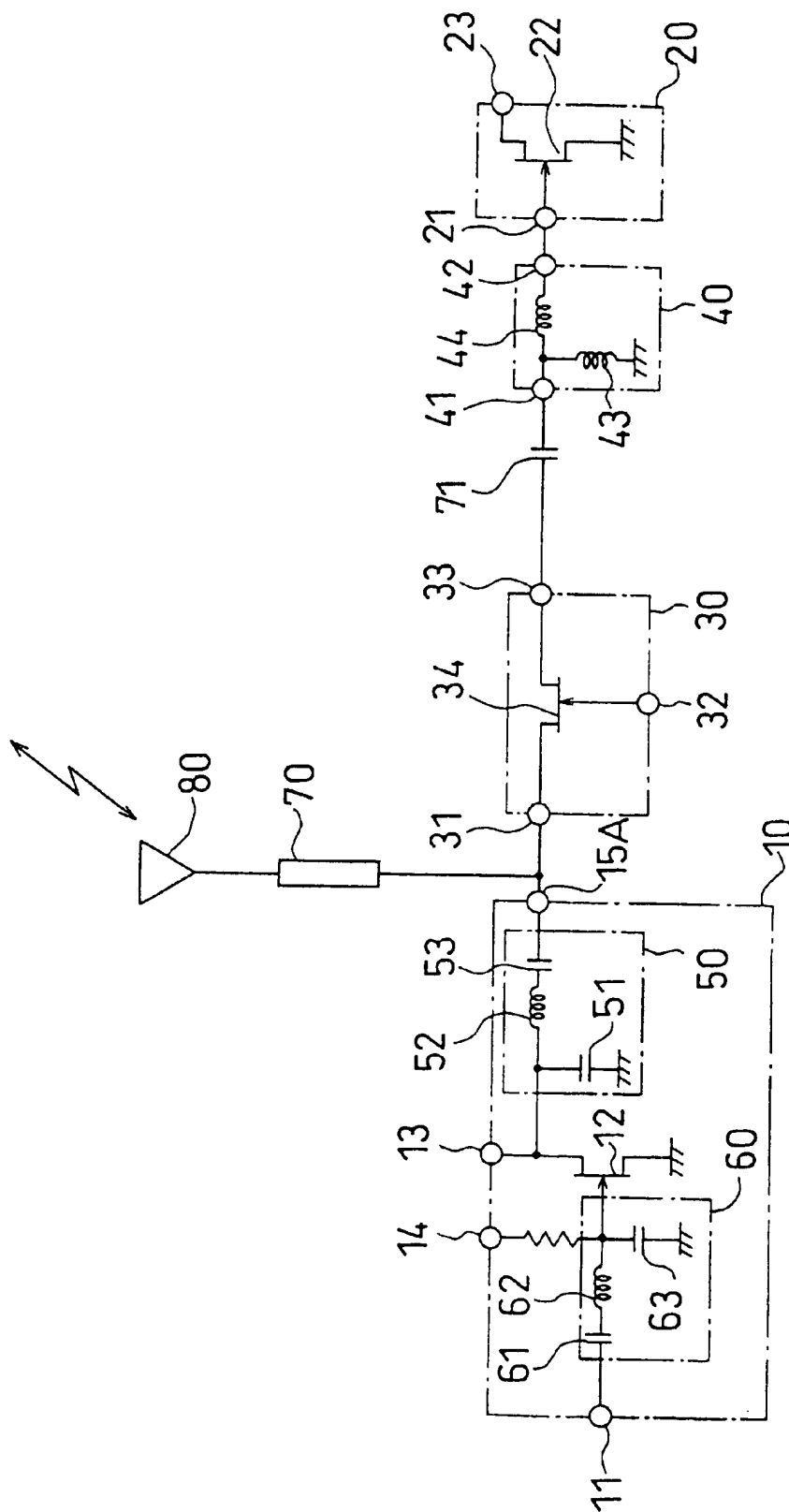
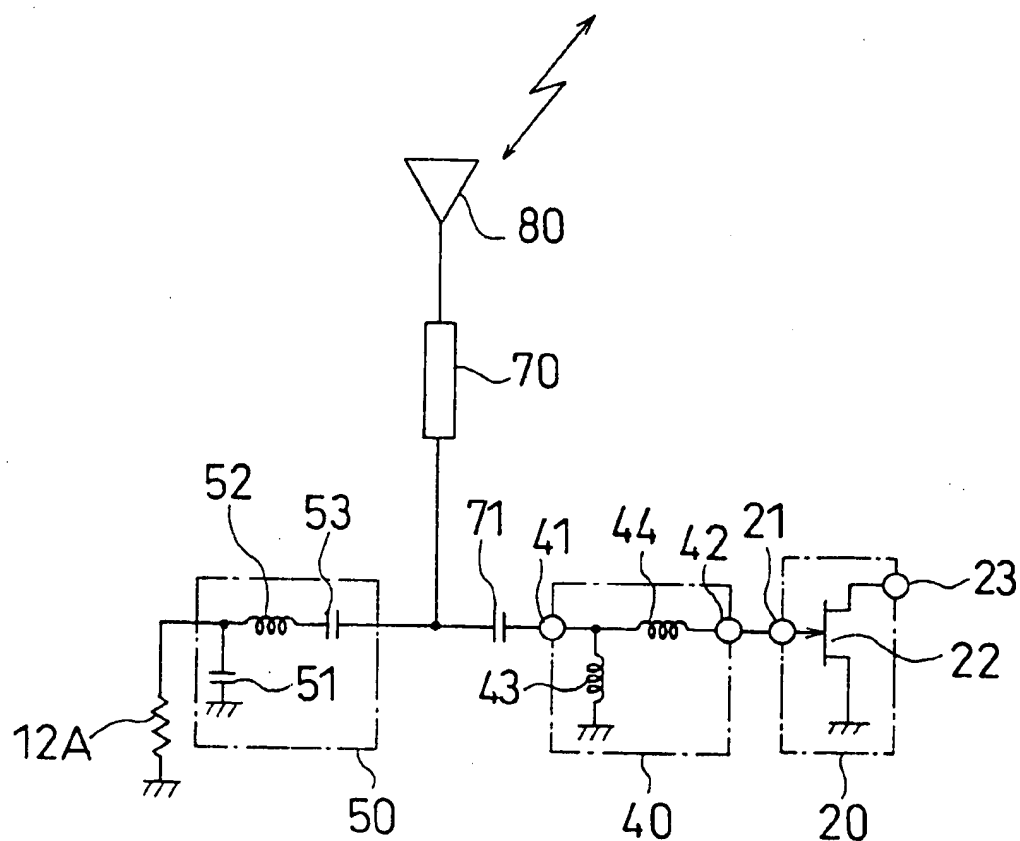


Fig. 2



Fi.
b.
3

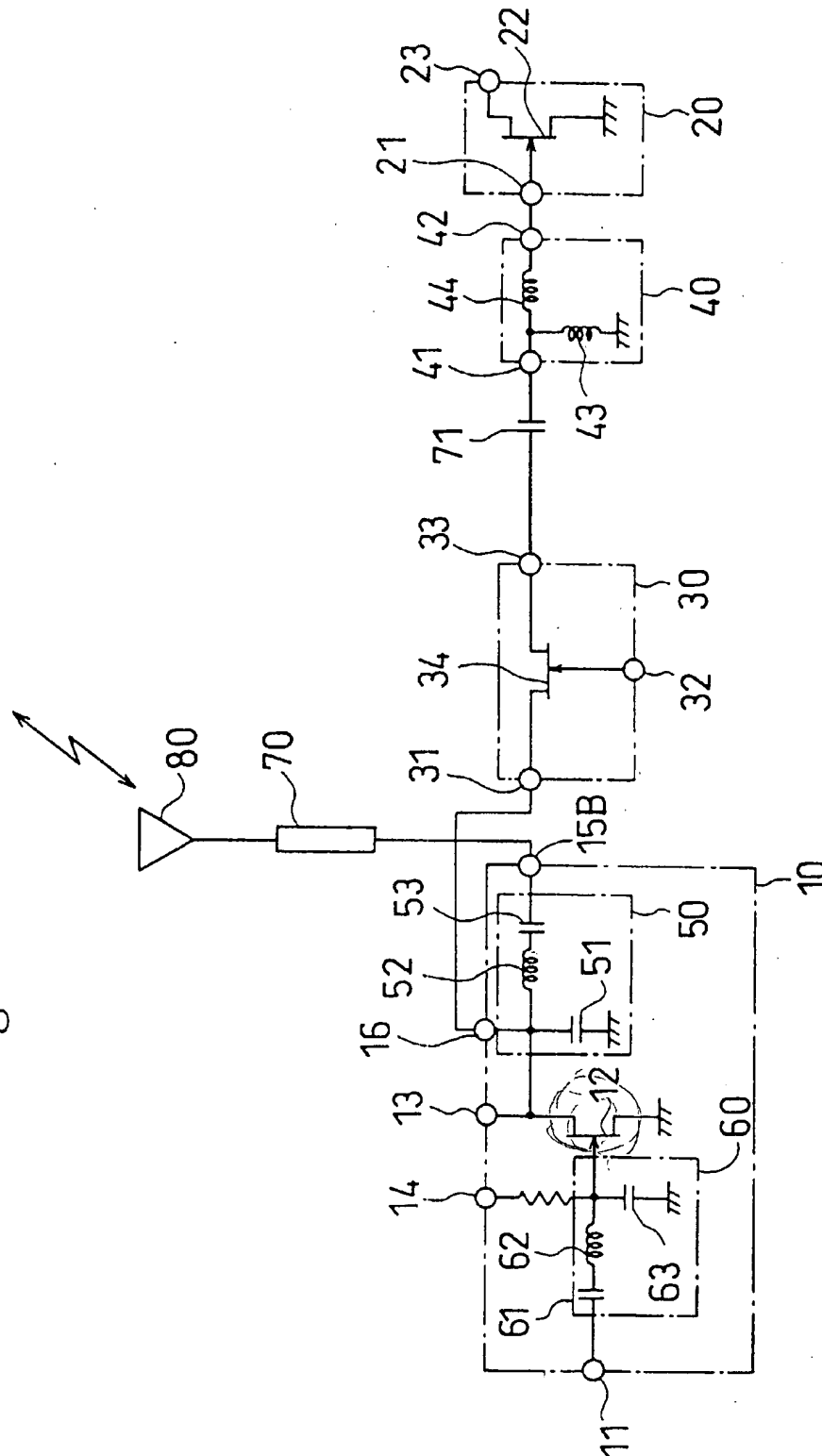


Fig. 4

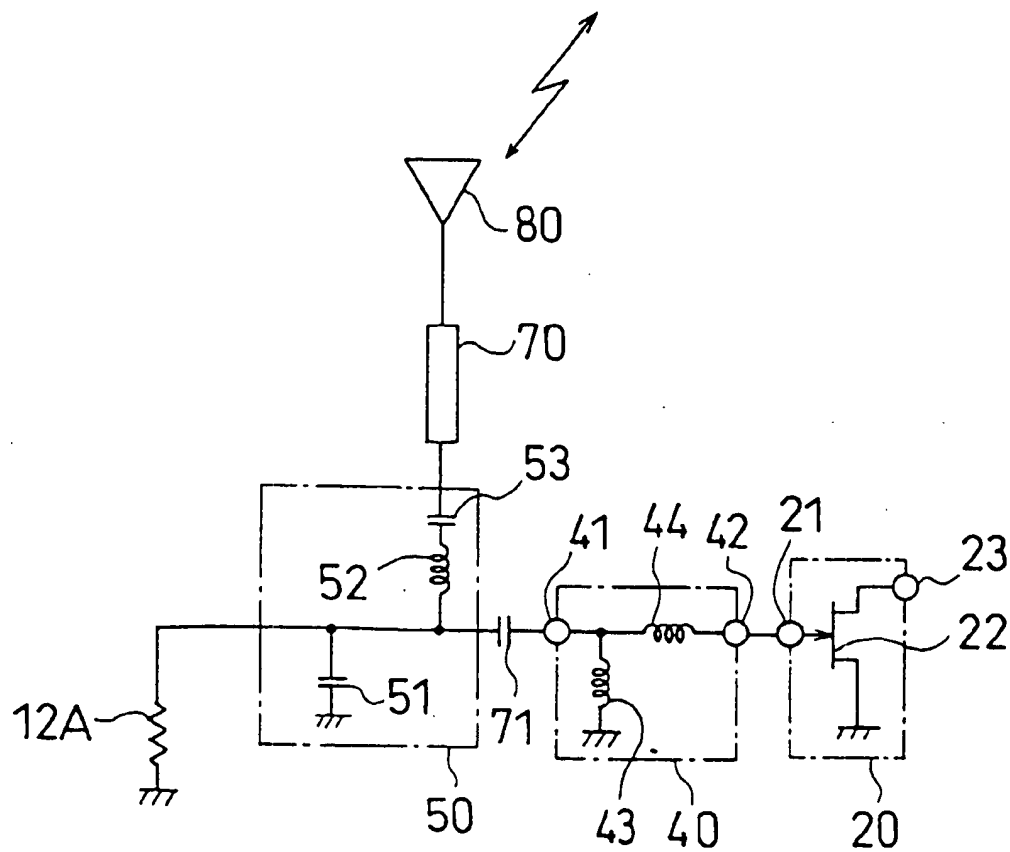


Fig. 5(a)

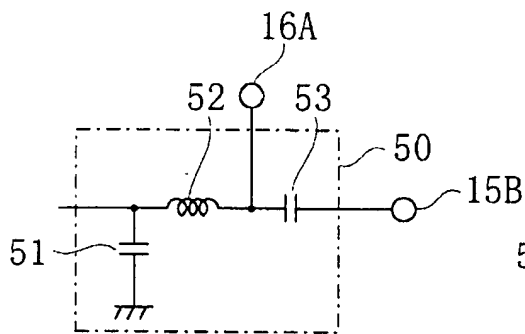


Fig. 5(b)

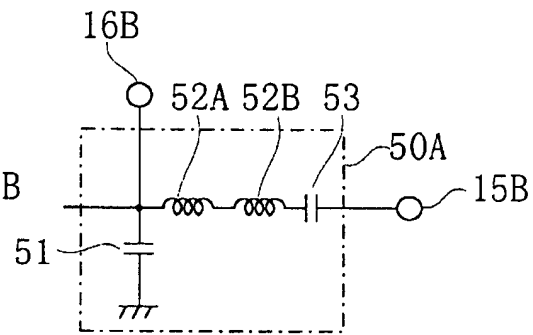


Fig. 5(c)

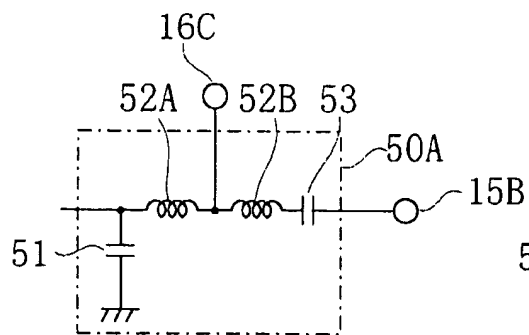


Fig. 5(d)

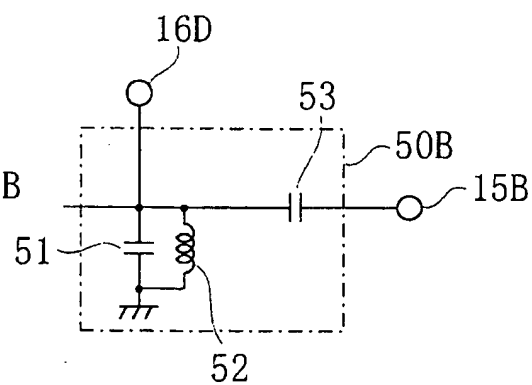


Fig. 6(a)

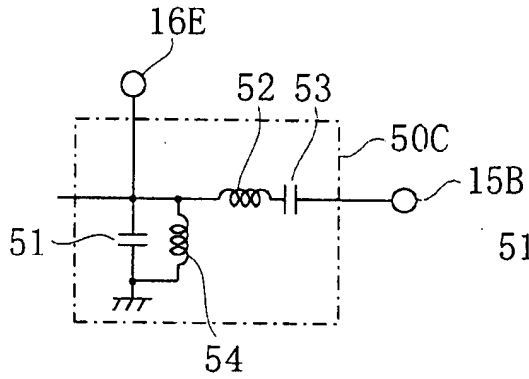


Fig. 6(b)

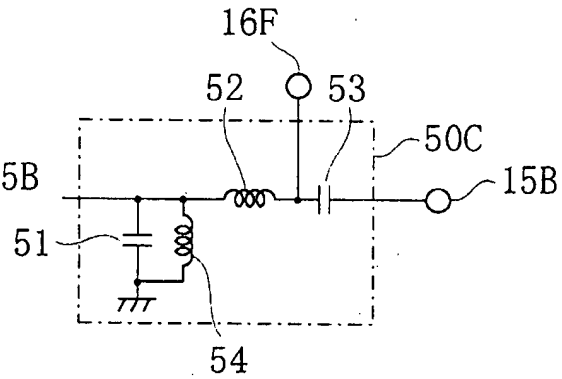


Fig. 6(c)

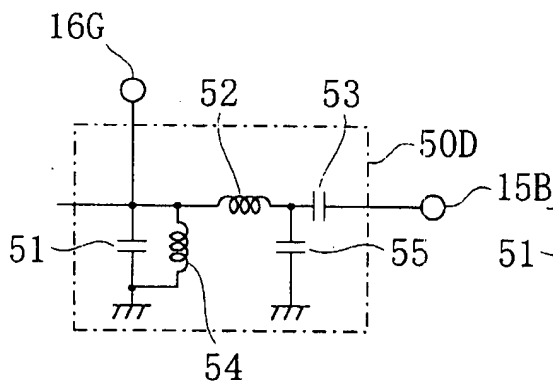


Fig. 6(d)

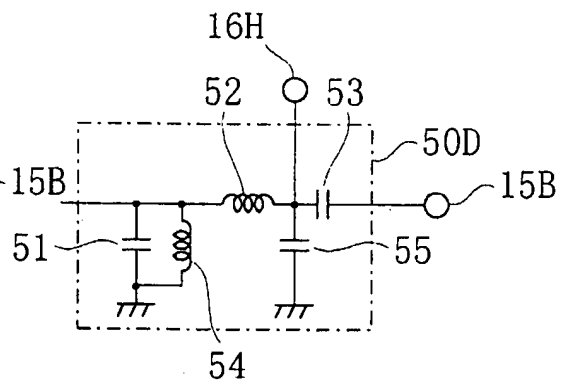


Fig. 7

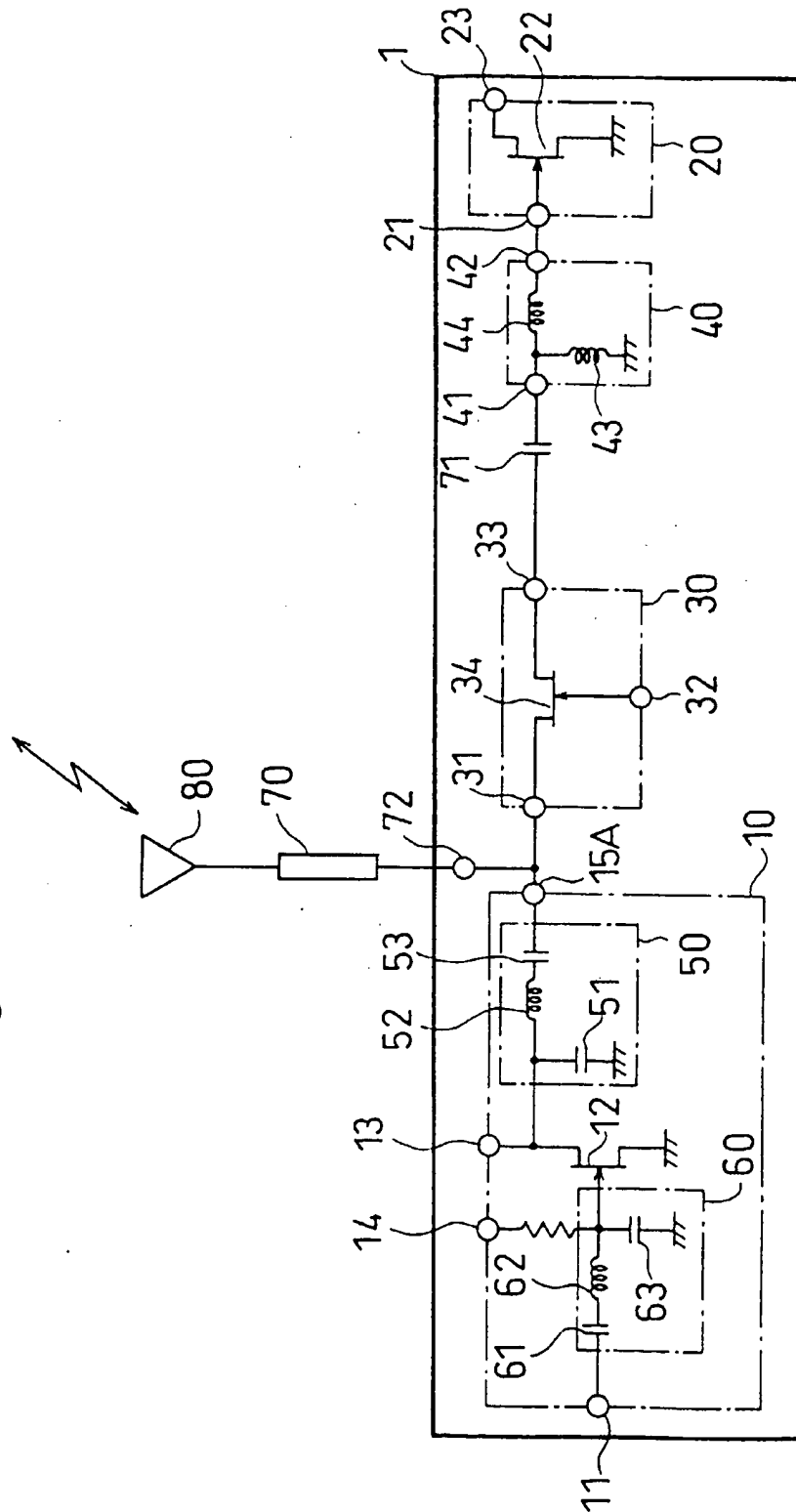


Fig. 8

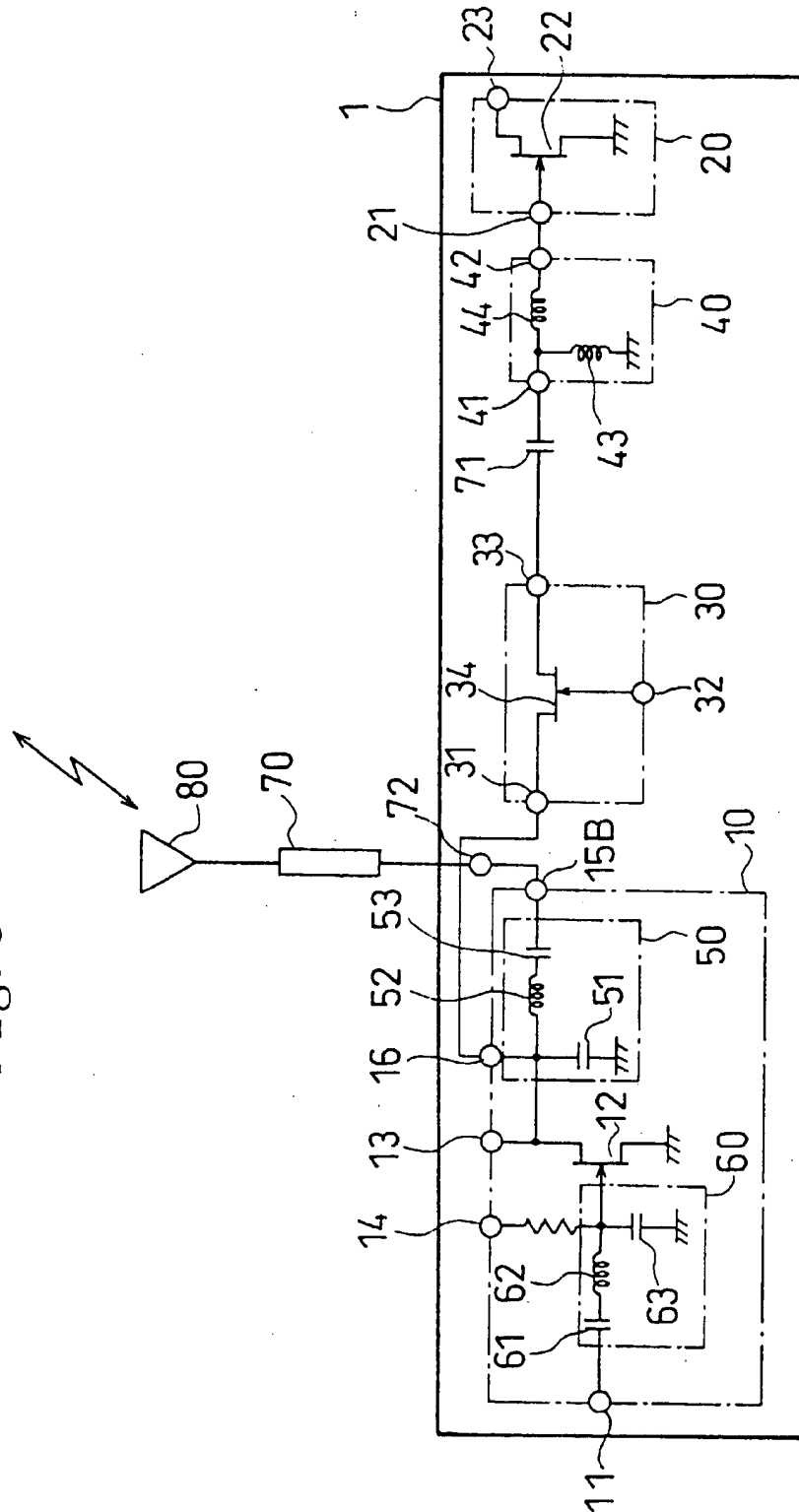


Fig. 9

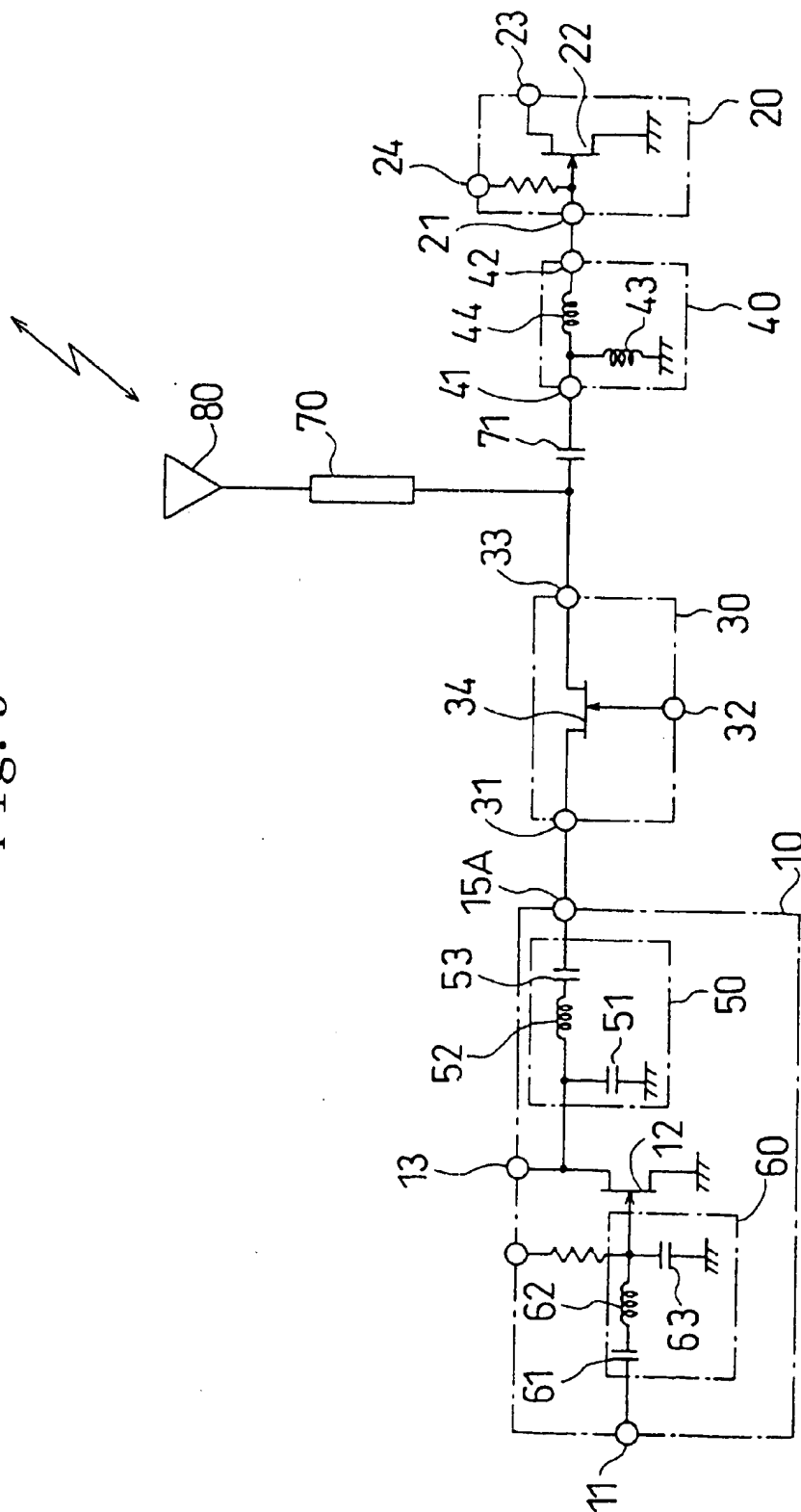


Fig. 10

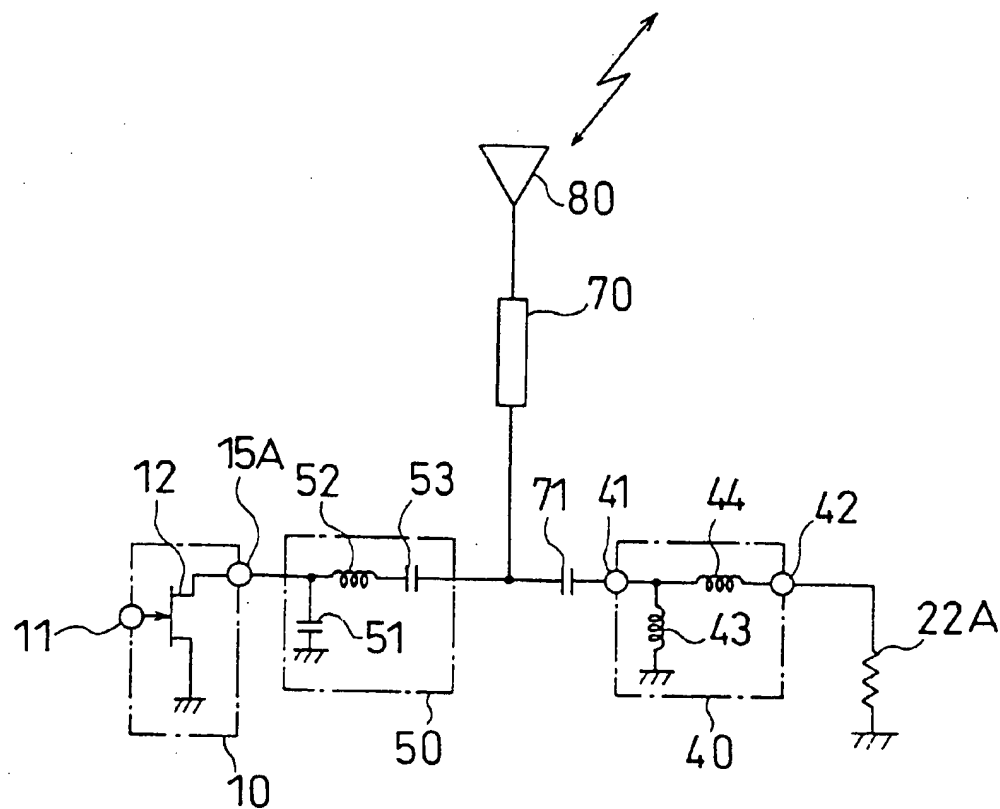
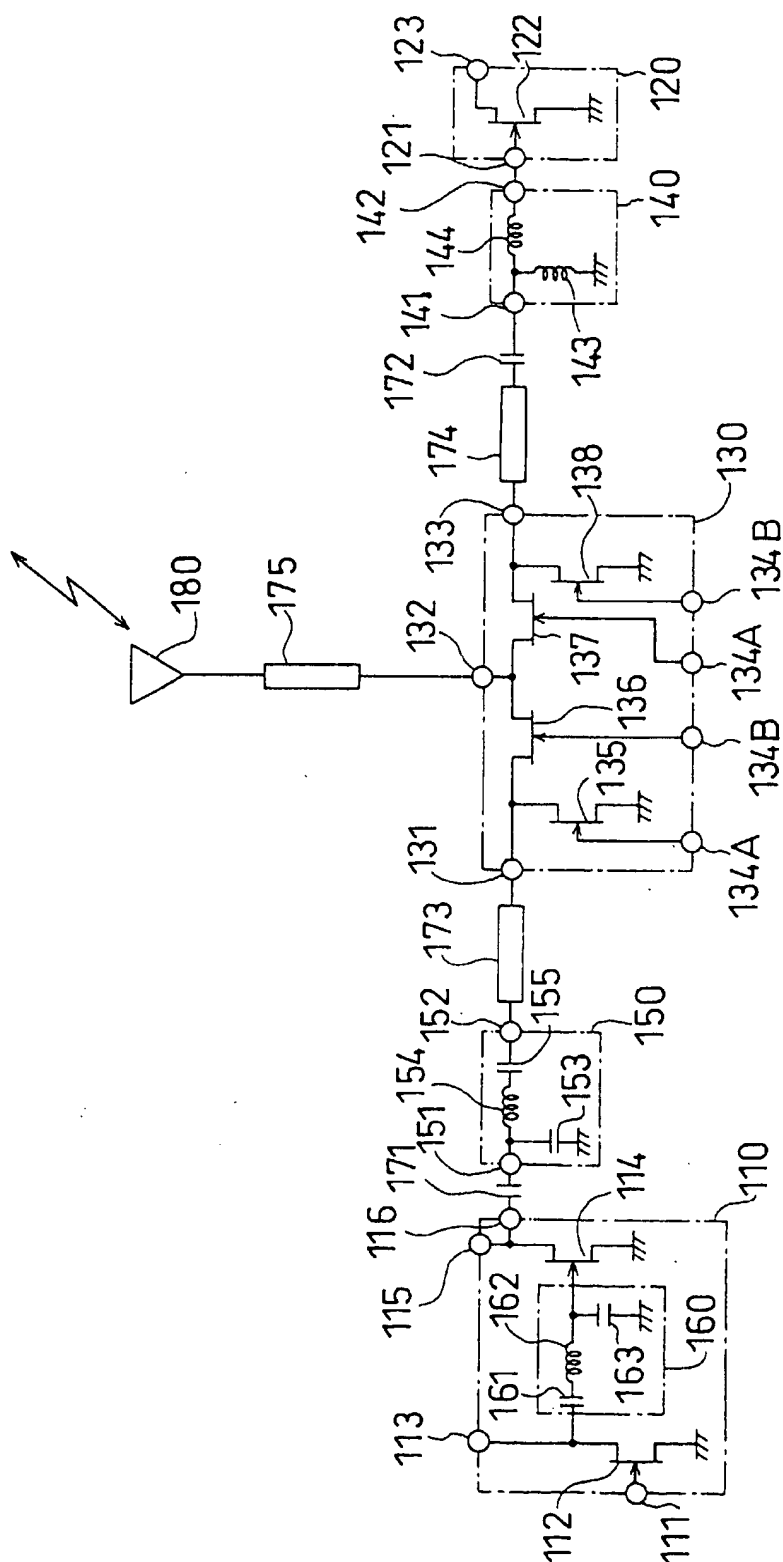


Fig. 11



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TRANSMITTER-RECEIVER CIRCUIT FOR RADIO COMMUNICATION AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

TECHNICAL FIELD

The present invention relates to a transmitter-receiver circuit and also relates to a semiconductor integrated circuit device including the transmitter-receiver circuit. More particularly, the present invention relates to transmitter-receiver circuit and semiconductor integrated circuit device suitable for a wireless communication unit using the same frequency as both transmission frequency and reception frequency.

BACKGROUND ART

In recent years, size, weight and price of various wireless communication units, e.g., portable cellular phone units for radio communication, have been drastically reduced, and the number of users thereof has been rapidly increasing. In conventional communication systems, a system configuration requiring distinct frequencies for transmission and reception has been adopted so far. On the other hand, in order to satisfy the needs of an even larger number of users, digital implementation has been gradually applied to these units. While two distinct frequencies per line have been required conventionally, such a digital wireless communication unit can perform transmission and reception with the same frequency by dividing transmission and reception in a time-division manner.

Even in such a wireless communication unit utilizing digital implementation, however, various circuits in a wireless circuit section, including a transmitter amplifier, a low-noise receiver amplifier and a transmission/reception mode switch for switching transmission and reception, are still implemented by conventional circuits. Thus, it is an important problem to develop downsized transmitter-receiver circuits and, in particular, semiconductor integrated circuit integrated with these circuits that are suitably applicable to brand-new digital implementation.

Also, a circuit including gallium-arsenide field effect transistors (hereinafter, simply referred to as "GaAs FETs"), having low-voltage, high-efficiency and low-noise operating characteristics and high-isolation characteristics, are often used for a transmitter amplifier, a low-noise receiver amplifier and a transmission/reception mode switch in a transmitter-receiver circuit for a wireless communication unit of a digital type.

Hereinafter, an example of a conventional transmitter-receiver circuit will be described with reference to the drawings.

FIG. 11 illustrates a configuration of a conventional digital transmitter-receiver circuit using FETs. In FIG. 11, 110 denotes a transmitter amplifier for amplifying an input signal to be transmitted and then outputting the amplified signal. 120 denotes a low-noise receiver amplifier for amplifying an input received signal and then outputting the amplified signal. 130 denotes a mode switch for switching transmission state and reception state in a time-division manner. 140 denotes a first matching circuit for matching the impedance of the input received signal with the input impedance of the low-noise receiver amplifier 120. 150 denotes a second matching circuit for matching the output impedance of the transmitter amplifier 110 with predetermined impedance. 160 denotes a third matching circuit for matching the output impedance of a FET 112 on the first

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stage with the input impedance of a FET on the second stage. 171 denotes first coupling capacitance for ac coupling the transmitter amplifier 110 with the second matching circuit 150. 172 denotes second coupling capacitance for ac coupling the mode switch 130 with the first matching circuit 140. 173 denotes a first interconnection, having characteristic impedance of 50Ω, for connecting the mode switch 130 to the second matching circuit 150. 174 denotes a second interconnection, having characteristic impedance of 50Ω, for connecting the mode switch 130 to the first matching circuit 140. 175 denotes a third interconnection, having characteristic impedance of 50Ω, for connecting the mode switch 130 to an antenna 180 used both for transmission and reception.

In the transmitter amplifier 110 shown in FIG. 11, 111 denotes an input terminal, through which a signal to be transmitted is input. 112 denotes a FET on the first stage, of which the gate electrode is provided with the input signal to be transmitted and the source is grounded. 113 denotes a first power supply terminal connected to the drain electrode of the FET 112 on the first stage. 114 denotes a FET on the second stage, of which the gate electrode is provided with the signal to be transmitted via the third matching circuit 160 and the source is grounded. 115 denotes a second power supply terminal connected to the drain electrode of the FET 114 on the second stage. 116 denotes an output terminal connected to the drain electrode of the FET 114 on the second stage.

In the low-noise receiver amplifier 120 shown in FIG. 11, 121 denotes an input terminal, through which a received signal is input via the first matching circuit 140. 122 denotes a low-noise FET, of which the gate electrode is provided with the received signal and the source is grounded. 123 denotes an output terminal connected to the drain electrode of the low-noise FET 122.

In the mode switch 130 shown in FIG. 11, 131 denotes an input terminal on the transmission side connected to the second matching circuit 150. 132 denotes an input/output terminal on the antenna side for outputting a signal to be transmitted, which has been amplified by the transmitter amplifier 110 and then input thereto via the second matching circuit 150 during transmission, to the antenna 180, and for receiving the received signal that has been received by the antenna 180 during reception. 133 denotes an output terminal on the reception side, through which the received signal input from the input/output terminal 132 on the antenna side is output. 134A denotes first switch-control-signal input terminals for controlling a first switching FET 135 and a third switching FET 137. 134B denotes second switch-control-signal input terminals for controlling a second switching FET 136 and a fourth switching FET 138.

In the first matching circuit 140 shown in FIG. 11, 141 denotes an input terminal connected to the output terminal 133 on the reception side of the mode switch 130 via the second coupling capacitance 172. 142 denotes an output terminal connected to the input terminal 121 of the low-noise receiver amplifier 120. 143 denotes a first inductor, one end of which is connected to the input terminal 141 and the other end of which is grounded, for constituting the first matching circuit 140. 144 denotes a second inductor, one end of which is connected to the input terminal 141 and the other end of which is connected to the output terminal 142, for constituting the first matching circuit 140.

In the second matching circuit 150 shown in FIG. 11, 151 denotes an input terminal connected to the output terminal 116 of the transmitter amplifier via the first coupling capaci-

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tance 171. 152 denotes an output terminal connected to the input terminal 131 on the transmission side of the mode switch 130. 153 denotes a first capacitor, one end of which is connected to the input terminal 151 and the other end of which is grounded, for constituting the second matching circuit 150. 154 denotes an inductor, one end of which is connected to the input terminal 151 and the other end of which is connected to a second capacitor 155, for constituting the second matching circuit 150. 155 denotes the second capacitor, one end of which is connected to the inductor 154 and the other end of which is connected to the output terminal 152, for constituting the second matching circuit 150.

In the third matching circuit 160 shown in FIG. 11, 161 denotes a first capacitor, one end of which is connected to the drain electrode of the FET 112 on the first stage in the transmitter amplifier 110 and the other end of which is connected to an inductor 162, for constituting the third matching circuit 160. 162 denotes the inductor, one end of which is connected to the first capacitor 161 and the other end of which is connected to the gate electrode of the FET 114 on the second stage in the transmitter amplifier 110, for constituting the third matching circuit 160. 163 denotes a second capacitor, one end of which is connected to the inductor 162 and the gate electrode of the FET 114 on the second stage and the other end of which is grounded, for constituting the third matching circuit 160.

Hereinafter, the operation of the transmitter-receiver circuit having the above-described configuration will be described.

First, the operation during reception will be described.

A less intense received signal, input via the antenna 180, passes through the third interconnection 175 having characteristic impedance of 50Ω and is input to the input/output terminal 132 on the antenna side of the mode switch 130. At this point in time, in the mode switch 130, the first switching FET 135 and the third switching FET 137 have been turned ON responsive to the control signal input through the first switch-control-signal input terminals 134A, while the second switching FET 136 and the fourth switching FET 138 have been turned OFF responsive to the control signal input through the second switch-control-signal input terminals 134B. Thus, the input signal is selectively directed to the low-noise receiver amplifier 120 via the third switching FET 137, which has been turned ON. On the other hand, the circuit section including the transmitter amplifier 110 is electrically isolated from the circuit section including the low-noise receiver amplifier 120, because the second switching FET 136 has been turned OFF. Also, the former circuit section is short-circuited, because the first switching FET 135 has been turned ON.

The signal switched by the third switching FET 137 in the conductive state is output through the output terminal on the reception side of the mode switch 130, passed through the second interconnection 174 having characteristic impedance of 50Ω and the second coupling capacitance 172 and then input to the first matching circuit 140. Then, impedance matching is performed by the first inductor 143 and the second inductor 144 of the first matching circuit 140. Thereafter, the signal is input to the input terminal 121 of the low-noise receiver amplifier 120. The received signal input to the low-noise receiver amplifier 120 is amplified by the low-noise FET 122 and the amplified signal is output through the output terminal 123.

Next, the operation during transmission will be described.

First, modulated signal to be transmitted is input to the input terminal 111 of the transmitter amplifier 110. Power

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amplification on the first stage is performed by the FET 112 on the first stage. Impedance conversion is performed by the third matching circuit 160. Then, the signal is input to the FET 114 on the second stage. The power of the signal is amplified by the FET 114 on the second stage so as to reach predetermined power. The amplified signal to be transmitted is input to the second matching circuit 150 via the first coupling capacitance 171. The characteristic impedance thereof is converted to be 50Ω . And then the signal is input to the input terminal 131 on the transmission side of the mode switch 130 through the first interconnection 173 having characteristic impedance of 50Ω .

At this point in time, in the mode switch 130, the second switching FET 136 and the fourth switching FET 138 have been turned ON responsive to the control signal input through the second switch-control-signal input terminals 134B, while the first switching FET 135 and the third switching FET 137 have been turned OFF responsive to the control signal input through the first switch-control-signal input terminals 134A. Thus, the input signal to be transmitted is selectively directed to the antenna 180 via the second switching FET 136, which has been turned ON. On the other hand, the circuit section including the low-noise receiver amplifier 120 is electrically isolated from the circuit section including the transmitter amplifier 110, because the third switching FET 137 has been turned OFF. Also, the former circuit section is short-circuited, because the fourth switching FET 138 has been turned ON.

The amplified signal to be transmitted passes through the second switching FET 136 in the conductive state and the third interconnection 175 having characteristic impedance of 50Ω and is input to the antenna 180 so as to be output through the antenna 180 as radio waves.

The above-described conventional transmitter-receiver circuit, however, had a problem in that the loss of a signal passing through the mode switch 130 is large. In particular, the loss of a signal to be transmitted becomes an issue because such a signal requires high power. Thus, it is necessary to improve the performance of a through-switching FET on the transmission side. In general, in order to reduce the pass loss, a switching FET having a large gate length is required. In addition, if switching FETs of such a large size are integrated, then the chip area is increased to such a degree that the area occupied by the mode switch 130 becomes substantially equal to the area of the transmitter amplifier 110. Thus, problems are present in that downsizing and cost-reduction thereof are hard to realize.

The present invention can solve the above-described conventional problems all at once, and has objects of reducing the power consumption by eliminating the pass loss caused by the mode switch on the signal to be transmitted and downsizing a wireless communication unit by reducing the area occupied by the mode switch in the transmitter-receiver circuit.

DISCLOSURE OF THE INVENTION

In order to accomplish the above-described objects, the present invention connects a transmitter amplifier to an antenna without interposing any mode switch therebetween by matching the inputs to a receiver amplifier while using, in combination, the output impedance of the transmitter amplifier during the OFF state and the output impedance to the receiver amplifier.

A transmitter-receiver circuit for a wireless communication unit according to the present invention includes: a transmitter amplifier for amplifying and outputting an input

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signal to be transmitted; a receiver amplifier for amplifying and outputting an input received signal; and a mode switch, connected to an antenna used for both transmission and reception, for switching a transmission state where the signal to be transmitted, which has been output by the transmitter amplifier, is output to the antenna and a reception state where the received signal, to be input to the receiver amplifier, is input through the antenna. The transmitter amplifier includes: an amplifying FET, having a gate electrode connected to an input terminal of the signal to be transmitted, a drain electrode connected to a power supply terminal and a source electrode grounded; a matching circuit, connected between the drain electrode of the FET and the antenna, for matching output impedance of the FET with impedance on the antenna side; a control terminal connected to the gate electrode of the FET; and an output terminal directly connected to the antenna without passing through the mode switch.

In the transmitter-receiver circuit for a wireless communication unit, since the output terminal of the transmitter amplifier is directly connected to the antenna without passing through the mode switch during transmission, the pass loss, ordinarily caused by a switch on a signal to be transmitted, can be eliminated. As a result, the power consumption can be reduced. On the other hand, during reception, since a control terminal connected to the gate electrode of the FET of the transmitter amplifier is provided, the circuit section on the transmission side is short-circuited by applying a predetermined voltage to the gate electrode and using the FET having the grounded source as resistance. As a result, a mode switch on the transmission side, which has conventionally been required, is no longer necessary. In other words, a mode switch on the reception side may be constituted by only one switching device, and thus the area occupied by the mode switch in the entire circuit can be reduced. As a result, the overall size of the transmitter-receiver circuit can be reduced.

Another transmitter-receiver circuit for a wireless communication unit according to the present invention includes: a transmitter amplifier for amplifying and outputting an input signal to be transmitted; a receiver amplifier for amplifying and outputting an input received signal; and a mode switch, connected to an antenna used for both transmission and reception, for switching a transmission state where the signal to be transmitted, which has been output by the transmitter amplifier, is output to the antenna and a reception state where the received signal, to be input to the receiver amplifier, is input through the antenna. The transmitter amplifier includes: an amplifying FET, having a gate electrode connected to an input terminal of the signal to be transmitted, a drain electrode connected to a power supply terminal and a source electrode grounded; a matching circuit, connected between the drain electrode of the FET and the antenna, for matching output impedance of the FET with impedance on the antenna side; a control terminal connected to the gate electrode of the FET; and an output terminal directly connected to the antenna without passing through the mode switch. The input terminal on the antenna side of the mode switch is connected to a terminal of the matching circuit, which is different from the output terminal of the signal to be transmitted of the matching circuit.

In the transmitter-receiver circuit for a wireless communication unit, since the output terminal of the transmitter amplifier is directly connected to the antenna without passing through the mode switch during transmission, the pass loss, ordinarily caused by a switch on a signal to be transmitted, can be eliminated. As a result, the power

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consumption can be reduced. On the other hand, during reception, since a control terminal connected to the gate electrode of the FET of the transmitter amplifier is provided, the circuit section on the transmission side is short-circuited by applying a predetermined voltage to the gate electrode and using the FET having the grounded source as resistance. As a result, a mode switch on the transmission side, which has conventionally been required, is no longer necessary. In other words, a mode switch on the reception side may be constituted by only one switching device, and thus the area occupied by the mode switch in the entire circuit can be reduced. As a result, the overall size of the transmitter-receiver circuit can be reduced. Moreover, where a receiving matching circuit for matching the impedance of the received signal with the input impedance of the receiver amplifier is provided between the mode switch and the receiver amplifier, a terminal allowing for optimization of the circuit constant of the receiving matching circuit can be selected. As a result, since the design flexibility of the receiving matching circuit can be increased, the size of the receiving matching circuit can be reduced.

A semiconductor integrated circuit device according to the present invention, includes: a semiconductor substrate; a transmitter amplifier, formed on the semiconductor substrate, for amplifying and outputting an input signal to be transmitted; a receiver amplifier, formed on the semiconductor substrate, for amplifying and outputting an input received signal; and a mode switch, formed on the semiconductor substrate and connected to an input/output terminal on an antenna side used for both transmission and reception, for switching a transmission state where the signal to be transmitted, which has been output by the transmitter amplifier, is output to the input/output terminal on the antenna side and a reception state where the received signal, to be input to the receiver amplifier, is input through the input/output terminal on the antenna side. The transmitter amplifier includes: an amplifying FET, having a gate electrode connected to an input terminal of the signal to be transmitted, a drain electrode connected to a power supply terminal and a source electrode grounded; a matching circuit, connected between the drain electrode of the FET and the input/output terminal on the antenna side, for matching output impedance of the FET with impedance on the antenna side; a control terminal connected to the gate electrode of the FET; and an output terminal directly connected to the input/output terminal on the antenna side without passing through the mode switch.

In the semiconductor integrated circuit device, since the output terminal of the transmitter amplifier is directly connected to the input/output terminal on the antenna side without passing through the mode switch during transmission, the pass loss, ordinarily caused by a switch on a signal to be transmitted, can be eliminated. As a result, the power consumption can be reduced. On the other hand, during reception, since a control terminal connected to the gate electrode of the FET of the transmitter amplifier is provided, the circuit section on the transmission side is short-circuited by applying a predetermined voltage to the gate electrode and using the FET as resistance. As a result, a mode switch on the reception side may be constituted by only one switching device, and thus the area occupied by the mode switch in the entire circuit can be reduced. Consequently, features advantageous for high integration can be attained and the device can be downsized.

Another semiconductor integrated circuit device according to the present invention includes: a semiconductor substrate; a transmitter amplifier, formed on the semicon-

ductor substrate, for amplifying and outputting an input signal to be transmitted; a receiver amplifier, formed on the semiconductor substrate, for amplifying and outputting an input received signal; and a mode switch, formed on the semiconductor substrate and connected to an input/output terminal on an antenna side used for both transmission and reception, for switching a transmission state where the signal to be transmitted, which has been output by the transmitter amplifier, is output to the input/output terminal on the antenna side and a reception state where the received signal, to be input to the receiver amplifier, is input through the input/output terminal on the antenna side. The transmitter amplifier includes: an amplifying FET, having a gate electrode connected to an input terminal of the signal to be transmitted, a drain electrode connected to a power supply terminal and a source electrode grounded; a matching circuit, connected between the drain electrode of the FET and the input/output terminal on the antenna side, for matching output impedance of the FET with impedance on the antenna side; a control terminal connected to the gate electrode of the FET; and an output terminal directly connected to the input/output terminal on the antenna side, without passing through the mode switch. The input terminal on the antenna side of the mode switch is connected to a terminal of the matching circuit, which is different from the output terminal of the signal to be transmitted of the matching circuit.

In the semiconductor integrated circuit device, since the output terminal of the transmitter amplifier is directly connected to the input/output terminal on the antenna side without passing through the mode switch during transmission, the pass loss, ordinarily caused by a switch on a signal to be transmitted, can be eliminated. As a result, the power consumption can be reduced. On the other hand, during reception, since a control terminal connected to the gate electrode of the FET of the transmitter amplifier is provided, the circuit section on the transmission side is short-circuited by applying a predetermined voltage to the gate electrode and using the FET as resistance. As a result, a mode switch on the transmission side is no longer necessary. In other words, a mode switch on the reception side may be constituted by only one switching device, and thus the area occupied by the mode switch in the entire circuit can be reduced. Moreover, where a receiving matching circuit for matching the impedance of the received signal with the input impedance of the receiver amplifier is provided between the mode switch and the receiver amplifier, a terminal allowing for optimization of the circuit constant of the receiving matching circuit can be selected. As a result, since the design flexibility of the receiving matching circuit can be increased, the size of the receiving matching circuit can be reduced. Consequently, the size of the device can be further reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a transmitter-receiver circuit for a wireless communication unit according to the first embodiment of the present invention.

FIG. 2 is an equivalent circuit diagram where the transmitter-receiver circuit for a wireless communication unit according to the first embodiment of the present invention performs receiving operation.

FIG. 3 is a circuit diagram of a transmitter-receiver circuit for a wireless communication unit according to the second embodiment of the present invention.

FIG. 4 is an equivalent circuit diagram where the transmitter-receiver circuit for a wireless communication

unit according to the second embodiment of the present invention performs receiving operation.

FIGS. 5(a) through 5(d) are circuit diagrams illustrating variations of a second matching circuit and an output terminal of a received signal in the transmitter-receiver circuit for a wireless communication unit according to the second embodiment of the present invention.

FIGS. 6(a) through 6(d) are circuit diagrams illustrating variations of the second matching circuit and the output terminal of the received signal in the transmitter-receiver circuit for a wireless communication unit according to the second embodiment of the present invention.

FIG. 7 is a circuit diagram of a transmitter-receiver circuit where GaAs FETs are used for a semiconductor integrated circuit device according to the third embodiment of the present invention.

FIG. 8 is a circuit diagram of a transmitter-receiver circuit where GaAs FETs are used for a semiconductor integrated circuit device according to the fourth embodiment of the present invention.

FIG. 9 is a circuit diagram of a transmitter-receiver circuit for a wireless communication unit according to the fifth embodiment of the present invention.

FIG. 10 is an equivalent circuit diagram where the transmitter-receiver circuit for a wireless communication unit according to the fifth embodiment of the present invention performs transmitting operation.

FIG. 11 is a circuit diagram of a conventional transmitter-receiver circuit of a digital type using FETs.

BEST MODE FOR CARRYING OUT THE INVENTION

First Embodiment

Hereinafter, the first embodiment of the present invention will be described with reference to the drawings.

FIG. 1 is a circuit diagram of a transmitter-receiver circuit for a wireless communication unit according to the first embodiment of the present invention. In FIG. 1, 10 denotes a transmitter amplifier for amplifying an input signal to be transmitted and then outputting the amplified signal. 20 denotes a low-noise receiver amplifier for amplifying an input received signal and then outputting the amplified signal. 30 denotes a mode switch for switching transmission state and reception state in a time-division manner. 40 denotes a first matching circuit for matching the impedance of the input received signal with the input impedance of the low-noise receiver amplifier 20. 50 denotes a second matching circuit for matching the output impedance of the transmitter amplifier 10 with predetermined impedance. 60 denotes a third matching circuit for matching the impedance of the input signal to be transmitted with the input impedance of a high-power FET 12 of the transmitter amplifier 10. 70 denotes an interconnection, having characteristic impedance of 50Ω, for connecting the mode switch 30, the transmitter amplifier 10 and an antenna 80 used for both transmission and reception with each other. 71 denotes coupling capacitance for ac coupling the mode switch 30 to the first matching circuit 40.

In the transmitter amplifier 10 shown in FIG. 1, 11 denotes an input terminal, through which a signal to be transmitted is input. 12 denotes a high-power FET, of which the gate electrode is provided with the input signal to be transmitted via the third matching circuit 60 and the source is grounded. 13 denotes a power supply terminal connected to the drain electrode of the high-power FET 12. 14 denotes a control terminal connected to the gate electrode of the high-power

FET 12 via resistance. 15A denotes an output terminal connected to the antenna 80 through an interconnection 70 having characteristic impedance of 50Ω and to an input terminal 31 of the mode switch 30.

In the low-noise receiver amplifier 20 shown in FIG. 1, 21 denotes an input terminal, through which a received signal is input via the first matching circuit 40. 22 denotes a low-noise FET, of which the gate electrode is provided with the received signal and the source is grounded. 23 denotes an output terminal connected to the drain electrode of the low-noise FET 22:

In the mode switch 30 shown in FIG. 1, 31 denotes an input terminal connected to the antenna 80 through the interconnection 70 having characteristic impedance of 50Ω and to the output terminal 15A of the transmitter amplifier 10. 32 denotes a switch-control-signal input terminal for controlling a switching FET 34. 33 denotes an output terminal, through which the received signal, input through the antenna 80, is output.

In the first matching circuit 40 shown in FIG. 1, 41 denotes an input terminal connected to the output terminal 33 of the mode switch 30 via the coupling capacitance 71. 42 denotes an output terminal connected to the input terminal 21 of the low-noise receiver amplifier 20. 43 denotes a first inductor, one end of which is connected to the input terminal 41 and the other end of which is grounded, for constituting the first matching circuit 40. 44 denotes a second inductor, one end of which is connected to the input terminal 41 and the other end of which is connected to the output terminal 42, for constituting the first matching circuit 40.

In the second matching circuit 50 shown in FIG. 1, 51 denotes a first capacitor, one end of which is connected to the drain electrode of the high-power FET 12 and the other end of which is grounded, for constituting the second matching circuit 50. 52 denotes an inductor, one end of which is connected to the drain electrode of the high-power FET 12 and the other end of which is connected to a second capacitor 53, for constituting the second matching circuit 50. 53 denotes a second capacitor, one end of which is connected to the inductor 52 and the other end of which is connected to the output terminal 15A, for constituting the second matching circuit 50.

In the third matching circuit 60 shown in FIG. 1, 61 denotes a first capacitor, one end of which is connected to the input terminal 11 of the transmitter amplifier 10 and the other end of which is connected to an inductor 62, for constituting the third matching circuit. 62 denotes the inductor, one end of which is connected to the first capacitor 61 and the other end of which is connected to the gate electrode of the high-power FET 12 of the transmitter amplifier 10, for constituting the third matching circuit 60. 63 denotes a second capacitor, one end of which is connected to the inductor 62 and the gate electrode of the high-power FET 12 and the other end of which is grounded, for constituting the third matching circuit.

In this embodiment, the FETs constituting the transmitter amplifier 10, the low-noise receiver amplifier 20 and the mode switch 30 are assumed to be GaAs FETs or silicon MOSFETs.

Hereinafter, the operation of the transmitter-receiver circuit having the above-described configuration will be described with reference to FIGS. 1 and 2.

FIG. 2 is an equivalent circuit diagram where the transmitter-receiver circuit for a wireless communication unit according to the first embodiment of the present invention performs receiving operation. In FIG. 2, the same

components as those of the transmitter-receiver circuit shown in FIG. 1 are identified by the same reference numerals and the description thereof will be omitted herein.

First, the operation thereof during reception will be described.

As shown in FIG. 1, a less intense received signal, which has been input through the antenna 80, passes through the interconnection 70 having characteristic impedance of 50Ω and is input to the mode switch 30.

In the mode switch 30, the switching FET 34 has been turned ON responsive to the control signal input through the switch-control-signal input terminal 32. Thus, the input received signal is next passed through the switching FET 34, the output terminal 33 of the mode switch 30 and the coupling capacitance 71 so as to be input to the first matching circuit 40.

Subsequently, the impedance of the input received signal is matched with the input impedance of the low-noise receiver amplifier 20. Thereafter, the signal is input to the input terminal 21 of the low-noise receiver amplifier 20. At this point in time, by turning ON the high-power FET 12 upon the application of a control voltage to the control terminal 14 of the high-power FET 12 in the transmitter amplifier 10, the high-power FET 12 can be equivalent to pure resistance 12A as shown in FIG. 2. Thus, the circuit section on the transmission can be short-circuited during reception. Accordingly, the input impedance of the low-noise receiver amplifier 20 can be matched by the first inductor 43 and the second inductor 44 constituting the first matching circuit 40 and the inductor 52 constituting the second matching circuit 50.

Next, the received signal input to the low-noise receiver amplifier 20 is amplified by the low-noise FET 22 and then output through the output terminal 23 of the low-noise receiver amplifier 20.

It is noted that, if the transmitter amplifier 10 performs multiple-stage amplification using a plurality of FETs, the control terminal 14 may be provided for the FET on the last amplification stage.

Next, the operation thereof during transmission will be described with reference to FIG. 1.

First, a signal to be transmitted, which has been modulated and amplified to reach a predetermined signal level, is input to the input terminal 11 of the transmitter amplifier 10.

Then, after the impedance of the input signal to be transmitted is matched by the third matching circuit 60 with the input impedance of the high-power FET 12, the input signal to be transmitted is amplified by the high-power FET 12 to gain predetermined power.

Subsequently, after having been subjected to the impedance conversion by the second matching circuit 50, the amplified signal to be transmitted is passed through the interconnection 70 having characteristic impedance of 50Ω, input to the antenna 80 and then output by the antenna 80 as radio waves. Since the switching FET 34 is turned OFF in the mode switch 30, the circuit section on the reception side is isolated from the antenna 80 and the transmitter amplifier 10.

This embodiment is characterized in that the transmitter amplifier 10 can be connected to the antenna 80 without interposing any switch therebetween by matching the inputs to the low-noise receiver amplifier 20 using the output impedance of the transmitter amplifier 10 during the OFF state and the output impedance of the first matching circuit 40 to the low-noise receiver amplifier 20. Thus, since the switch for transmission need not be used, the pass loss caused by a switching device on the output signal of the

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transmitter amplifier 10 can be eliminated. As a result, low power consumption is realized during transmission.

In addition, since only one switching FET is necessary, the mode switch can have a reduced area and can be integrated more highly.

The value of resistance where the control terminal 14 of the high-power FET 12 is used as having been turned ON by applying a voltage to the control terminal 14 during the transmission OFF state is equal to or lower than 1Ω , which is the ON resistance of a generally used FET. Thus, the influence of the resistance on the input matching of the low-noise receiver amplifier 20 is negligible.

Second Embodiment

Hereinafter, the second embodiment of the present invention will be described with reference to the drawings.

FIG. 3 is a circuit diagram of a transmitter-receiver circuit for a wireless communication unit according to the second embodiment of the present invention. In FIG. 3, 10 denotes a transmitter amplifier for amplifying an input signal to be transmitted and then outputting the amplified signal. 20 denotes a low-noise receiver amplifier for amplifying an input received signal and then outputting the amplified signal. 30 denotes a mode switch for switching transmission state and reception state in a time-division manner. 40 denotes a first matching circuit for matching the impedance of the input received signal with the input impedance of the low-noise receiver amplifier 20. 50 denotes a second matching circuit for matching the output impedance of the transmitter amplifier 10 with predetermined impedance. 60 denotes a third matching circuit for matching the impedance of the input signal to be transmitted with the input impedance of a high-power FET 12 of the transmitter amplifier 10. 70 denotes an interconnection, having characteristic impedance of 50Ω , for connecting a terminal 15B functioning as output terminal for transmission and input terminal for reception of the transmitter amplifier 10 to the antenna 80 used for both transmission and reception. 71 denotes coupling capacitance for ac coupling the mode switch 30 to the first matching circuit 40. In FIG. 3, the same components as those of the circuits shown in FIG. 1 are identified by the same reference numerals and the description thereof will be omitted herein.

This embodiment is different from the first embodiment in that the input terminal 31 of the mode switch 30 is connected not to the terminal 15B functioning as output terminal for transmission and input terminal for reception of the transmitter amplifier 10, but to an output terminal 16 of the received signal. The output terminal 16 is used in common both as a terminal of the drain electrode of the high-power FET 12 and as a non-grounded terminal of the first capacitor 51 in the second matching circuit 50.

Hereinafter, the operation of the transmitter-receiver circuit having the above-described configuration will be described with reference to FIGS. 3 and 4.

The operation thereof during transmission is the same as that of the transmitter-receiver circuit described in the first embodiment, and thus the description thereof will be omitted herein. Only the operation thereof during reception will be described hereinafter.

FIG. 4 is an equivalent circuit diagram where the transmitter-receiver circuit for a wireless communication unit according to the second embodiment performs receiving operation.

First, as shown in FIG. 3, a less intense received signal, which has been input through the antenna 80, passes through the interconnection 70 having characteristic impedance of 50Ω , the terminal 15B functioning as output terminal for

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transmission and input terminal for reception of the transmitter amplifier 10 and the second matching circuit 50, and then is input to the mode switch 30.

In the mode switch 30, the switching FET 34 has been turned ON responsive to the control signal input through the switch-control-signal input terminal 32. Thus, the input received signal is next passed through the switching FET 34, the output terminal 33 of the mode switch 30 and the coupling capacitance 71 so as to be input to the first matching circuit 40.

Subsequently, the impedance of the input received signal is matched with the input impedance of the low-noise receiver amplifier 20 by the first matching circuit 40. Thereafter, the signal is input to the input terminal 21 of the low-noise receiver amplifier 20. At this point in time, by turning ON the high-power FET 12 upon the application of a control voltage to the control terminal 14 of the high-power FET 12 in the transmitter amplifier 10, the high-power FET 12 can be equivalent to pure resistance 12A as shown in FIG. 4. Thus, the circuit section on the transmission side can be short-circuited during reception. Accordingly, the input impedance of the low-noise receiver amplifier 20 can be matched by the first inductor 43 and the second inductor 44 constituting the first matching circuit 40 and the inductor 52 constituting the second matching circuit 50.

Next, the received signal input to the low-noise receiver amplifier 20 is amplified by the low-noise FET 22 and then output through the output terminal 23 of the low-noise receiver amplifier 20.

It is noted that, if the transmitter amplifier 10 performs multiple-stage amplification using a plurality of FETs, the control terminal 14 may be provided for the FET on the last amplification stage.

As can be understood, in this second embodiment, the resulting number of devices can be reduced, for example, by using the inductor 43 required for the first matching circuit 40 simultaneously as the inductor 52 in the second matching circuit 50 as shown in FIG. 4. As a result, the size of the first matching circuit 40 can be reduced.

That is to say, during reception, there is no problem if only impedance matching is realized between the antenna 80 and the low-noise receiver amplifier 20 by using the devices of the first matching circuit 40 and the second matching circuit. Thus, by comparison to the first embodiment, the design flexibility of the first matching circuit 40 can be increased.

For example, once the first matching circuit 40 is fixed, the first matching circuit 40 itself cannot be changed. However, even in such a case, by providing the output terminal 16 of the received signal at such a position of the second matching circuit 50 as to optimize the impedance matching with the low-noise receiver amplifier 20, the first matching circuit 40 can also be connected to the output terminal 16 of the received signal. Thus, the number of devices can be reduced simultaneously.

Herein, variations of the second matching circuit 50 and variations of the output terminal of the received signal at respective positions corresponding to the respective variations where impedance matching with the low-noise receiver amplifier 20 is optimized are illustrated in FIGS. 5 and 6. In the second matching circuit 50 shown in FIG. 5(a), the output terminal 16A of the received signal is connected to the connection point between the inductor 52 and the second capacitor 53. In the second matching circuit 50A shown in FIG. 5(b), the inductor is divided into two parts 52A and 52B, and the output terminal 16B of the received signal is connected to the drain electrode of a high-power FET 12

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(not shown) and to a non-grounded terminal, i.e., a common terminal of the first capacitor 51. In the second matching circuit 50A shown in FIG. 5(c), the output terminal 16C of the received signal is connected to a common terminal of the inductors 52A and 52B. In the second matching circuit 50B shown in FIG. 5(d), one terminal of the inductor 52 is grounded and the other end thereof is connected to the drain electrode of the high-power FET 12 and to the non-grounded terminal, i.e., the common terminal of the first capacitor 51, to which terminal the output terminal 16D of the received signal is connected. In the second matching circuit 50C shown in FIG. 6(a), a second inductor 54 is newly added to the second matching circuit 50, one terminal of the second inductor 54 is grounded and the other end thereof is connected to the drain electrode of the high-power FET 12 and to the non grounded terminal, i.e., the common terminal of the first capacitor 51, to which terminal the output terminal 16E of the received signal is connected. In the second matching circuit 50C shown in FIG. 6(b), the output terminal 16F of the received signal is connected to the connection point between the inductor 52 and the second capacitor 53. In the second matching circuit 50D shown in FIG. 6(c), a third capacitor 55 is newly added to the second matching circuit 50C, one terminal of the third capacitor 55 is grounded and the other end thereof is connected to the connection point between the inductor 52 and the second capacitor 53, and the output terminal 16G of the received signal is connected to the drain electrode of a high-power FET 12 (not shown) and to a non-grounded terminal, i.e., a common terminal of the first capacitor 51. In the second matching circuit 50D shown in FIG. 6(d), the output terminal 16H of the received signal is connected to a common connection point among the inductor 52, the second capacitor 53 and the third capacitor 55.

Third Embodiment

Hereinafter, the third embodiment of the present invention will be described with reference to the drawings.

FIG. 7 is a circuit diagram of a transmitter-receiver circuit where GaAs FETs are used for a semiconductor integrated circuit device according to the third embodiment of the present invention. That is to say, FIG. 7 is a circuit diagram of a device formed by integrating the transmitter-receiver circuit for a wireless communication unit as described in the first embodiment onto a semiconductor substrate.

In FIG. 7, 10 denotes a transmitter amplifier for amplifying an input signal to be transmitted and then outputting the amplified signal. 20 denotes a low-noise receiver amplifier for amplifying an input received signal and then outputting the amplified signal. 30 denotes a mode switch for switching transmission state and reception state in a time-division manner. 40 denotes a first matching circuit for matching the impedance of the input received signal with the input impedance of the low-noise receiver amplifier 20. 50 denotes a second matching circuit for matching the output impedance of the transmitter amplifier 10 with predetermined impedance. 60 denotes a third matching circuit for matching the impedance of the input signal to be transmitted with the input impedance of a high-power FET 12 of the transmitter amplifier 10. 70 denotes an interconnection, having characteristic impedance of 50Ω , for connecting an input/output terminal 72 on the antenna side to the antenna 80 used for both transmission and reception. 71 denotes coupling capacitance for ac coupling the mode switch 30 to the first matching circuit 40.

The respective circuits described above, i.e., the transmitter amplifier 10 including the second matching circuit 50 and the third matching circuit 60, the low-noise receiver

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amplifier 20, the mode switch 30 and the first matching circuit 40, are formed on a semiconductor substrate

In the transmitter amplifier 10 shown in FIG. 7, 11 denotes an input terminal, through which a signal to be transmitted is input. 12 denotes a high-power FET, of which the gate electrode is provided with the input signal to be transmitted via the third matching circuit 60 and the source is grounded. 13 denotes a power supply terminal connected to the drain electrode of the high-power FET 12. 14 denotes a control terminal connected to the gate electrode of the high-power FET 12. 15A denotes a terminal functioning as output terminal on the transmission side and input terminal on the reception side, which is connected to the input/output terminal 72 on the antenna side and to the input terminal 31 of the mode switch 30.

In the low-noise receiver amplifier 20 shown in FIG. 7, 21 denotes an input terminal of the low-noise receiver amplifier 20, through which a received signal is input via the first matching circuit 40. 22 denotes a low-noise FET, of which the gate electrode is provided with the received signal and the source is grounded. 23 denotes an output terminal of the low-noise receiver amplifier 20 connected to the drain electrode of the low-noise FET 22.

In the mode switch 30 shown in FIG. 7, 31 denotes an input terminal connected to the antenna 80 through the interconnection 70 having characteristic impedance of 50Ω and to the output terminal 15 of the transmitter amplifier 10. 32 denotes a switch-control-signal input terminal for controlling a switching FET. 33 denotes an output terminal, through which the received signal, input through the antenna 80, is output. 34 denotes a switching FET constituting the mode switch 30. In FIG. 7, the same components as those of the respective matching circuits shown in FIG. 1 are identified by the same reference numerals and the description thereof will be omitted herein.

Since the operation of the semiconductor integrated circuit device according to this embodiment is the same as that of the first embodiment, the description thereof will be omitted herein.

In accordance with this embodiment, the transmitter amplifier 10 can be connected to the antenna 80 without interposing any switch therebetween by matching the inputs to the low-noise receiver amplifier 20 while using, in combination, the output impedance of the transmitter amplifier 10 during the OFF state and the output impedance of the first matching circuit 40 to the low-noise receiver amplifier 20. Thus, since the use of a switch for transmission is no longer necessary, it is possible to eliminate the pass loss that is ordinarily caused by a switching device on the output signal of the transmitter amplifier 10. As a result, the power consumption can be reduced during transmission.

In addition, since only one switching FET is required, the area occupied by the mode switch on the transmitter-receiver circuit can be narrowed, high integration is enabled. Ultimately, this fact can contribute to downsizing and cost reduction of a wireless communication unit incorporating the semiconductor integrated circuit device according to this embodiment.

In this embodiment, GaAs FETs are used as the FETs constituting the transmitter amplifier 10, the low-noise receiver amplifier 20 and the mode switch 30. Alternatively, these FETs may be silicon MOSFETs.

The value of resistance where the control terminal 14 of the high-power FET 12 is used as having been turned ON by applying a voltage to the control terminal 14 during the transmission OFF state is equal to or lower than 10, which is the ON resistance of a generally used FET. Thus, the

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influence of the resistance on the input matching of the low-noise receiver amplifier 20 is negligible.

Fourth Embodiment

Hereinafter, the fourth embodiment of the present invention will be described with reference to the drawings.

FIG. 8 is a circuit diagram of a transmitter-receiver circuit where GaAs FETs are used for a semiconductor integrated circuit device according to the fourth embodiment of the present invention. That is to say, FIG. 8 is a circuit diagram of a device formed by integrating the transmitter-receiver circuit for a wireless communication unit as described in the second embodiment onto a semiconductor substrate.

In FIG. 8, 10 denotes a transmitter amplifier for amplifying an input signal to be transmitted and then outputting the amplified signal. 20 denotes a low-noise receiver amplifier for amplifying an input received signal and then outputting the amplified signal. 30 denotes a mode switch for switching transmission state and reception state in a time-division manner. 40 denotes a first matching circuit for matching the impedance of the input received signal with the input impedance of the low-noise receiver amplifier 20. 50 denotes a second matching circuit for matching the output impedance of the transmitter amplifier 10 with predetermined impedance. 60 denotes a third matching circuit for matching the impedance of the input signal to be transmitted with the input impedance of a high-power FET 12 of the transmitter amplifier 10. 70 denotes an interconnection, having characteristic impedance of 50Ω , for connecting an input/output terminal 72 on the antenna side to the antenna 80 used for both transmission and reception. 71 denotes coupling capacitance for ac coupling the mode switch 30 to the first matching circuit 40. It is noted that the same components as those of the respective circuits shown in FIG. 3 are identified by the same reference numerals and the description thereof will be omitted herein.

The respective circuits described above, i.e., the transmitter amplifier 10 including the second matching circuit 50 and the third matching circuit 60, the low-noise receiver amplifier 20, the mode switch 30 and the first matching circuit 40, are formed on a semiconductor substrate 1.

The fourth embodiment is characterized in that the input terminal 31 of the mode switch 30 is not connected to the terminal 15B functioning as output terminal for transmission and input terminal for reception of the transmitter amplifier 10, but to the output terminal 16 of the received signal in the second matching circuit 50.

The operations thereof during reception and transmission are the same as those of the transmitter-receiver circuit as described in the second embodiment. Thus, the description thereof will be omitted herein.

In accordance with the fourth embodiment, by turning ON the high-power FET 12 upon the application of a control voltage to the control terminal 14 of the high-power FET 12 in the transmitter amplifier 10 shown in FIG. 8 and by using the high-power FET 12 as pure resistance 12A, the circuit section on the transmission side can be short-circuited and isolated during reception.

Thus, the resulting number of devices can be reduced by using the inductor required for the first matching circuit 40 simultaneously as the inductor 52 in the second matching circuit 50 as shown in FIG. 8. As a result, the size of the first matching circuit 40 can be reduced.

That is to say, during reception, there is no problem if only impedance matching is realized between the antenna 80 and the low-noise receiver amplifier 20 by using the devices of the first matching circuit 40 and the second matching circuit. Thus, by comparison to the third embodiment, the design

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flexibility of the first matching circuit 40 can be increased. For example, by providing the output terminal 16 of the received signal at such a position of the second matching circuit 50 as to optimize the impedance matching with the low-noise receiver amplifier 20, the input terminal 31 of the mode switch 30 can also be connected to the output terminal 16 of the received signal. Thus, the number of devices can be reduced simultaneously. In this case, it is naturally possible to apply the respective variations 50A through 50D of the second matching circuit 50 shown in FIGS. 5 and 6 and the respective variations of the output terminals 16A to 16H of the received signal corresponding to the respective variations.

In addition, since only one switching FET is required, the area occupied by the mode switch 30 and the first matching circuit 40 on the transmitter-receiver circuit can be narrowed, high integration is realized more easily. Ultimately, this fact can contribute more to downsizing and cost reduction of a wireless communication unit incorporating the semiconductor integrated circuit device according to this embodiment.

Fifth Embodiment

Hereinafter, the fifth embodiment of the present invention will be described with reference to the drawings.

FIG. 9 is a circuit diagram of a transmitter-receiver circuit for a wireless communication unit according to the fifth embodiment of the present invention.

The fifth embodiment is characterized by the configuration in which the transmission/reception mode switch is not connected between the antenna and the low-noise receiver amplifier as is done in the foregoing embodiments, but is connected between the antenna and the transmitter amplifier. In FIG. 9, 10 denotes a transmitter amplifier for amplifying an input signal to be transmitted and then outputting the amplified signal. 20 denotes a low-noise receiver amplifier for amplifying an input received signal and then outputting the amplified signal. 30 denotes a mode switch for switching transmission state and reception state in a time-division manner. 40 denotes a first matching circuit for matching the impedance of the input received signal with the input impedance of the low-noise receiver amplifier 20. 50 denotes a second matching circuit for matching the output impedance of the transmitter amplifier 10 with predetermined impedance. 60 denotes a third matching circuit for matching the impedance of the input signal to be transmitted with the input impedance of a high-power FET 12 of the transmitter amplifier 10. 70 denotes an interconnection, having characteristic impedance of 50Ω , for connecting the mode switch 30, the first matching circuit 40 and an antenna 80 used for both transmission and reception to each other. 71 denotes coupling capacitance for ac coupling the mode switch 30 to the first matching circuit 40.

In the transmitter amplifier 10 shown in FIG. 9, 11 denotes an input terminal, through which a signal to be transmitted is input. 12 denotes a high-power FET, of which the gate electrode is provided with the input signal to be transmitted via the third matching circuit 60 and the source is grounded. 13 denotes a power supply terminal connected to the drain electrode of the high-power FET 12. 15A denotes an output terminal connected to the input terminal 31 of the mode switch 30.

In the low-noise receiver amplifier 20 shown in FIG. 9, 21 denotes an input terminal, through which a received signal is input via the coupling capacitance 71 and the first matching circuit 40. 22 denotes a low-noise FET, of which the gate electrode is provided with the received signal and the source is grounded. 23 denotes an output terminal connected to the

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drain electrode of the low-noise FET 22. 24 denotes a control terminal connected to the gate electrode of the low-noise FET 22.

In the mode switch 30 shown in FIG. 9, 31 denotes an input terminal connected to the output terminal 15 of the transmitter amplifier 10. 32 denotes a switch-control-signal input terminal for controlling a switching FET. 33 denotes an output terminal, through which the amplified signal to be transmitted is output to the antenna 80. 34 denotes a switching FET constituting the mode switch 30.

In the first matching circuit 40 shown in FIG. 9, 41 denotes an input terminal connected to the antenna 80 and to the output terminal 33 of the mode switch 30 via the coupling capacitance 71 and an interconnection having characteristic impedance of 50Ω . 42 denotes an output terminal connected to the input terminal 21 of the low-noise receiver amplifier 20. 43 denotes a first inductor, one end of which is connected to the input terminal 41 of the first matching circuit 40 and the other end of which is grounded, for constituting the first matching circuit 40. 44 denotes a second inductor, one end of which is connected to the input terminal 41 of the first matching circuit 40 and the other end of which is connected to the output terminal 42, for constituting the first matching circuit 40.

In the second matching circuit 50 shown in FIG. 1, 51 denotes a first capacitor, one end of which is connected to the drain electrode of the high-power FET and the other end of which is grounded, for constituting the second matching circuit 50. 52 denotes an inductor, one end of which is connected to the drain electrode of the high-power FET and the other end of which is connected to a second capacitor 53, for constituting the second matching circuit 50. 53 denotes a second capacitor, one end of which is connected to the inductor 52 and the other end of which is connected to the output terminal 15A of the transmitter amplifier 10, for constituting the second matching circuit 50.

All of the FETs constituting the transmitter amplifier 10, the low-noise receiver amplifier 20 and the mode switch 30 of this transmitter-receiver circuit are assumed to be GaAs FETs or silicon MOSFETs.

Hereinafter, the operation of the transmitter-receiver circuit having the above-described configuration will be described with reference to FIGS. 9 and 10.

FIG. 10 is an equivalent circuit diagram where the transmitter-receiver circuit for a wireless communication unit according to the fifth embodiment of the present invention performs transmitting operation. In FIG. 10, the same components as those of the transmitter-receiver circuit shown in FIG. 9 are identified by the same reference numerals and the description thereof will be omitted herein.

First, the operation thereof during reception will be described.

A less intense received signal, which has been input through the antenna 80, passes through the interconnection 70 having characteristic impedance of 50Ω and is input to the first matching circuit 40 shown in FIG. 9 via the coupling capacitance 71.

Subsequently, the impedance of the input received signal is matched with the input impedance of the low-noise receiver amplifier 20 by the first matching circuit 40. Thereafter, the signal is input to the input terminal 21 of the low-noise receiver amplifier 20. The input received signal is amplified by the low-noise FET 22 and then output through the output terminal 23 of the low-noise receiver amplifier 20. Since the switching FET 34 has been turned OFF in the mode switch 30, the circuit section on the transmission side is isolated from the antenna 80 and the low-noise receiver amplifier 20.

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Next, the operation thereof during transmission will be described.

First, a signal to be transmitted, which has been modulated and amplified to reach a predetermined signal level, is input to the input terminal 11 of the transmitter amplifier 10.

Then, after the impedance of the input signal to be transmitted is matched by the third matching circuit 60 with the input impedance of the high-power FET 12, the input signal to be transmitted is amplified by the high-power FET 12 to gain desired power.

At this point in time, by turning ON the low-noise FET 22 upon the application of a positive voltage, which is equal to larger than Schottky voltage, to the control terminal 24 of the low-noise FET 22 in the low-noise receiver amplifier 20 shown in FIG. 9, the low-noise FET 22 can be equivalent to pure resistance 22A as shown in FIG. 10. Thus, the circuit section on the reception side can be short-circuited during transmission. Accordingly, the output impedance of the transmitter amplifier 10 can be matched with predetermined impedance by the first inductor 43 and the second inductor 44 constituting the first matching circuit 40 and the inductor 52 constituting the second matching circuit 50.

Next, the signal to be transmitted, subjected to the impedance matching, passes through the interconnection 70 having characteristic impedance of 50Ω and is input to the antenna 80 so as to be output through the antenna 80 as radio waves.

It is noted that the impedance matching should be performed between the first matching circuit and the second matching circuit so that the amplified signal to be transmitted does not flow toward the low-noise receiver amplifier 20.

As can be understood from the above description, in the fifth embodiment, the outputs of the transmitter amplifier 10 are matched by using, in combination, the impedance of the low-noise receiver amplifier 20 during the OFF state and the impedance of the second matching circuit 50 in the transmitter amplifier 10 whereby the low-noise receiver amplifier 20 can be connected to the antenna 80 without interposing any switch. As a result, since a switch for reception can be omitted, it is possible to eliminate the pass loss, which is ordinarily caused by a switch on the input signal of the low-noise receiver amplifier 20.

Furthermore, since the less intense received signal is not attenuated, the S/N ratio during amplification can be increased. Moreover, since only one switching FET is enough, a switch can be downsized and highly integrated.

INDUSTRIAL APPLICABILITY

As is apparent from the foregoing description, in the transmitter-receiver circuit for a wireless communication unit according to the present invention, the output terminal of the transmitter amplifier is directly connected to the antenna without passing through the mode switch during transmission. Thus, the pass loss, ordinarily caused by a switch on a signal to be transmitted, can be eliminated. As a result, the power consumption can be reduced. On the other hand, during reception, the circuit section on the transmission side is short-circuited by using the FET for transmission amplification as resistance. As a result, a mode switch on the transmission side is no longer necessary. In other words, a mode switch on the reception side may be constituted by only one switching device, and thus the area occupied by the mode switch in the entire circuit can be reduced. Consequently, the overall size of the transmitter-receiver circuit can be reduced.

On the other hand, since the semiconductor integrated circuit device according to the present invention is consti-

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tuted by the transmitter-receiver circuit for a wireless communication unit according to the present invention, the power consumption during transmission can be reduced and the overall size of the transmitter-receiver circuit can be reduced. Thus, the present invention is advantageous for even higher integration. As a result, the costs of a semiconductor integrated circuit device can be reduced.

What is claimed is:

1. A transmitter-receiver circuit for a wireless communication unit, comprising:

- a transmitter amplifier for amplifying and outputting an input signal to be transmitted;
- a receiver amplifier for amplifying and outputting an input received signal; and
- a mode switch, connected to an antenna used for both transmission and reception, for switching a transmission state where the signal to be transmitted, which has been output by the transmitter amplifier, is output to the antenna and a reception state where the received signal, to be input to the receiver amplifier, is input through the antenna,

characterized in that the transmitter amplifier includes:

- an amplifying FET, having a gate electrode connected to an input terminal of the signal to be transmitted, a drain electrode connected to a power supply terminal and a source electrode grounded;
- a matching circuit, connected between the drain electrode of the FET and the antenna, for matching output impedance of the FET with impedance on an antenna side;
- a control terminal connected to the gate electrode of the FET; and
- an output terminal directly connected to the antenna without passing through the mode switch.

2. A transmitter-receiver circuit for a wireless communication unit, comprising:

- a transmitter amplifier for amplifying and outputting an input signal to be transmitted;
- a receiver amplifier for amplifying and outputting an input received signal; and
- a mode switch, connected to an antenna used for both transmission and reception, for switching a transmission state where the signal to be transmitted, which has been output by the transmitter amplifier, is output to the antenna and a reception state where the received signal, to be input to the receiver amplifier, is input through the antenna,

characterized in that the transmitter amplifier includes:

- an amplifying FET, having a gate electrode connected to an input terminal of the signal to be transmitted, a drain electrode connected to a power supply terminal and a source electrode grounded;
- a matching circuit, connected between the drain electrode of the FET and the antenna, for matching output impedance of the FET with impedance on an antenna side;
- a control terminal connected to the gate electrode of the FET; and
- an output terminal directly connected to the antenna without passing through the mode switch,

and that an input terminal on the antenna side of the mode switch is connected to a terminal of the matching circuit, which is different from an output terminal of the signal to be transmitted of the matching circuit.

3. A semiconductor integrated circuit device, comprising:
a semiconductor substrate;

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a transmitter amplifier, formed on the semiconductor substrate, for amplifying and outputting an input signal to be transmitted;

a receiver amplifier, formed on the semiconductor substrate, for amplifying and outputting an input received signal; and

a mode switch, formed on the semiconductor substrate and connected to an input/output terminal on an antenna side used for both transmission and reception, for switching a transmission state where the signal to be transmitted, which has been output by the transmitter amplifier, is output to the input/output terminal on the antenna side and a reception state where the received signal, to be input to the receiver amplifier, is input through the input/output terminal on the antenna side,

characterized in that the transmitter amplifier includes:

- an amplifying FET, having a gate electrode connected to an input terminal of the signal to be transmitted, a drain electrode connected to a power supply terminal and a source electrode grounded;
- a matching circuit, connected between the drain electrode of the FET and the input/output terminal on the antenna side, for matching output impedance of the FET with impedance on the antenna side;
- a control terminal connected to the gate electrode of the FET; and
- an output terminal directly connected to the input/output terminal on the antenna side without passing through the mode switch.

4. A semiconductor integrated circuit device, comprising:

- a semiconductor substrate;
- a transmitter amplifier, formed on the semiconductor substrate, for amplifying and outputting an input signal to be transmitted;
- a receiver amplifier, formed on the semiconductor substrate, for amplifying and outputting an input received signal; and
- a mode switch, formed on the semiconductor substrate and connected to an input/output terminal on an antenna side used for both transmission and reception, for switching a transmission state where the signal to be transmitted, which has been output by the transmitter amplifier, is output to the input/output terminal on the antenna side and a reception state where the received signal, to be input to the receiver amplifier, is input through the input/output terminal on the antenna side,

characterized in that the transmitter amplifier includes:

- an amplifying FET, having a gate electrode connected to an input terminal of the signal to be transmitted, a drain electrode connected to a power supply terminal and a source electrode grounded;
 - a matching circuit, connected between the drain electrode of the FET and the input/output terminal on the antenna side, for matching output impedance of the FET with impedance on the antenna side;
 - a control terminal connected to the gate electrode of the FET; and
 - an output terminal directly connected to the input/output terminal on the antenna side without passing through the mode switch,
- and that an input terminal on the antenna side of the mode switch is connected to a terminal of the matching circuit, which is different from an output terminal of the signal to be transmitted of the matching circuit.

* * * * *



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United States Patent [19]

Itoh et al.

[11] Patent Number: **5,784,687**[45] Date of Patent: **Jul. 21, 1998**

[54] **TRANSMITTING-RECEIVING CIRCUIT FOR RADIOCOMMUNICATION APPARATUS, SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING THE CIRCUIT, AND RADIOCOMMUNICATION APPARATUS INCLUDING THE SAME**

[75] Inventors: **Junji Itoh; Kazuhisa Fujimoto**, both of Osaka, Japan

[73] Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka, Japan

[21] Appl. No.: **520,676**

[22] Filed: **Aug. 29, 1995**

[30] **Foreign Application Priority Data**

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Mar. 9, 1995 [JP] Japan 7-049474

[51] Int. Cl.⁶ **H04B 1/48**

[52] U.S. Cl. **455/78; 455/82; 455/83; 333/103; 333/126**

[58] Field of Search **455/78, 80, 82, 455/83, 84, 89, 90, 129; 333/101, 103, 104, 118, 124, 126, 132**

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Primary Examiner—Reinhard J. Eisenzopf

Assistant Examiner—Thanh Le

Attorney, Agent, or Firm—McDermott, Will & Emery

[57]

ABSTRACT

A changeover switch switches connection between an antenna and a transmitter amplifier and connection between the antenna and a receiver low noise amplifier, from one to the other. A first wire having characteristic impedance of 50 Ω connects the antenna and the changeover switch. A receiver matching circuit matches input impedance of the receiver low noise amplifier with the output impedance of the transmitter amplifier. An antenna side matching circuit matches the input impedance of the receiver low noise amplifier, which is matched with the output impedance of the transmitter amplifier by the receiver matching circuit, and the output impedance of the transmitter amplifier with the characteristic impedance of the first wire. The transmitter amplifier is connected with the changeover switch via a first coupling capacitance, and the receiver matching circuit is connected with the changeover switch via a second coupling capacitance.

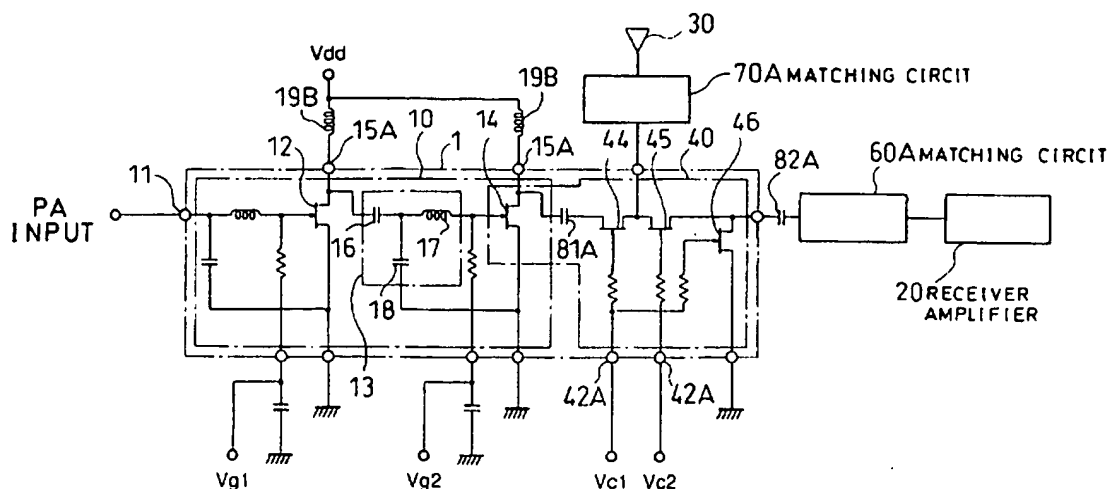
8 Claims, 8 Drawing Sheets

FIG. 1 (a)
PRIOR ART

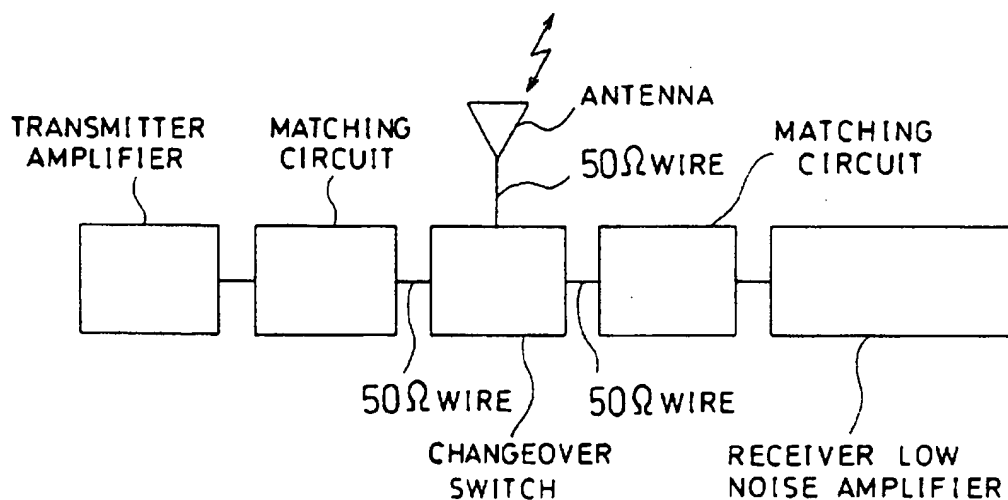


FIG. 1 (b)

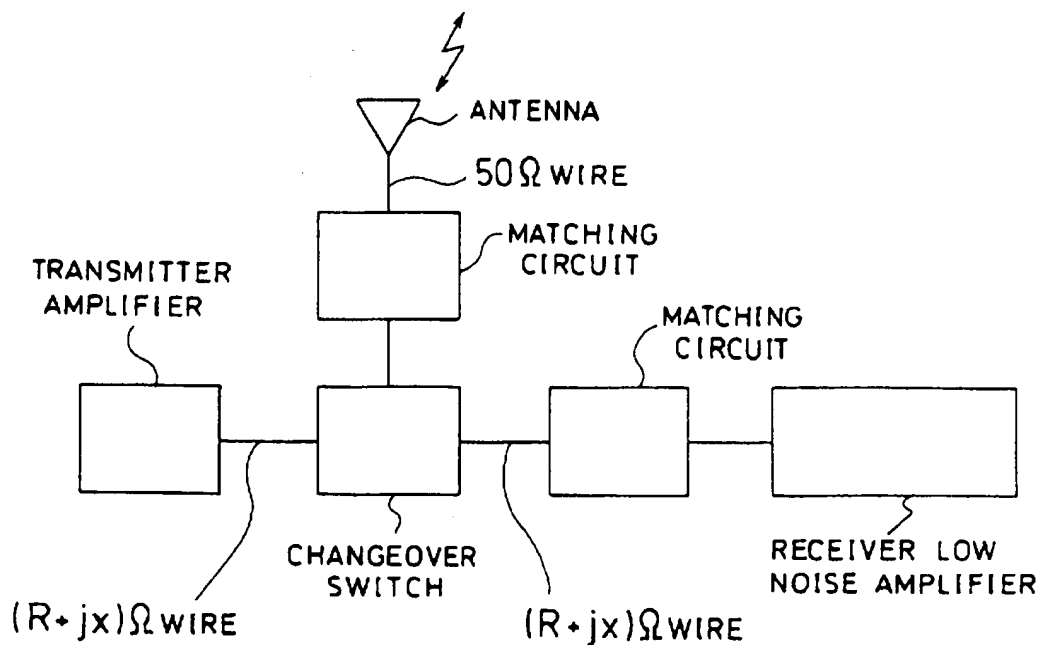


FIG. 2

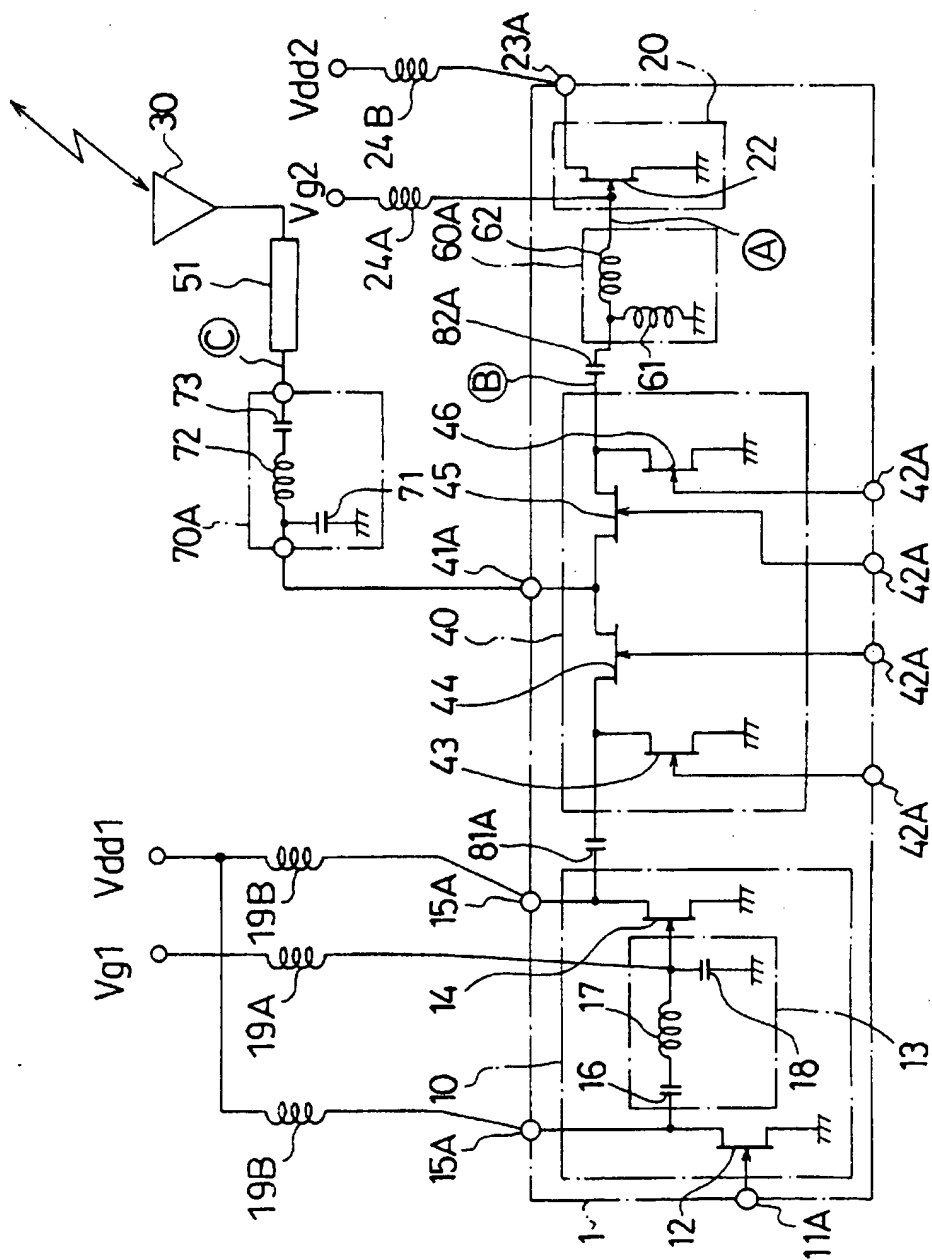


FIG. 3

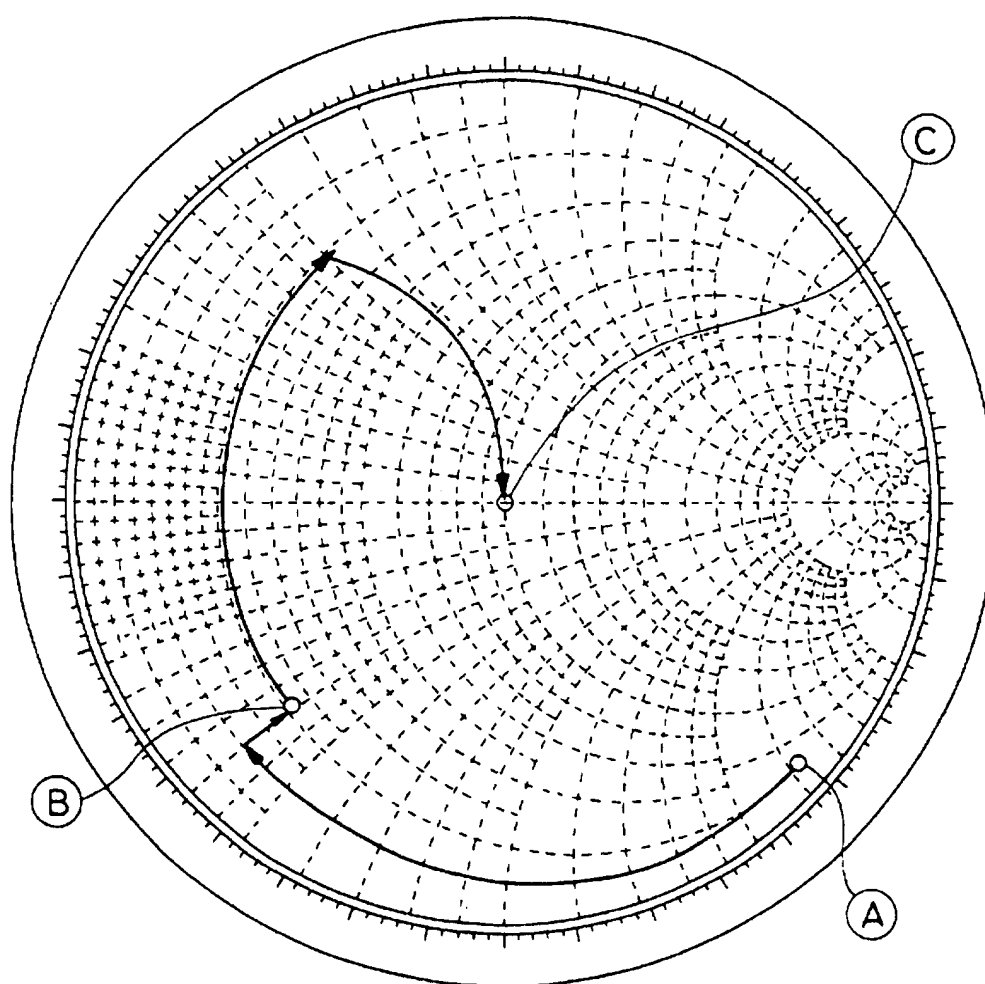


FIG. 4

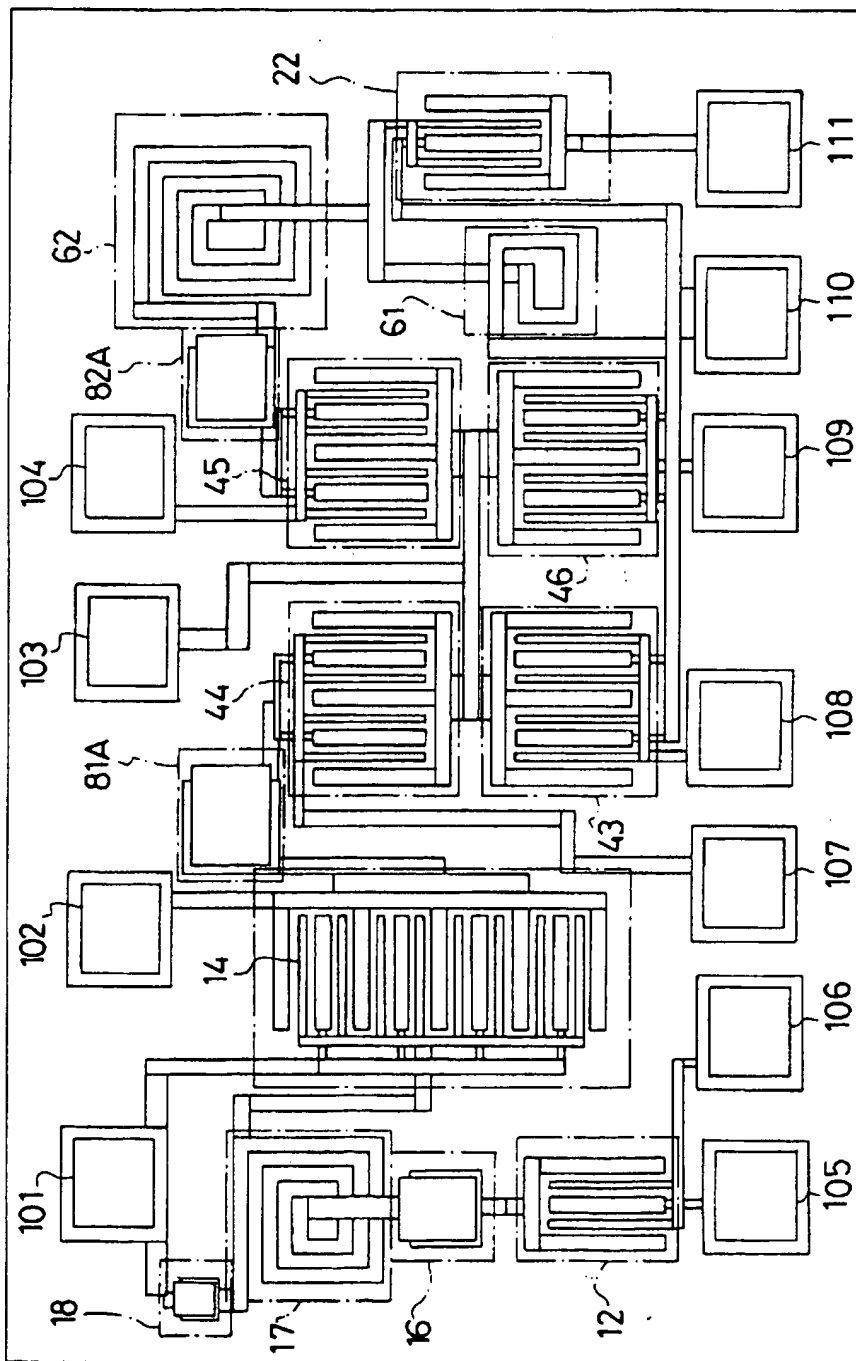


FIG. 5(a)

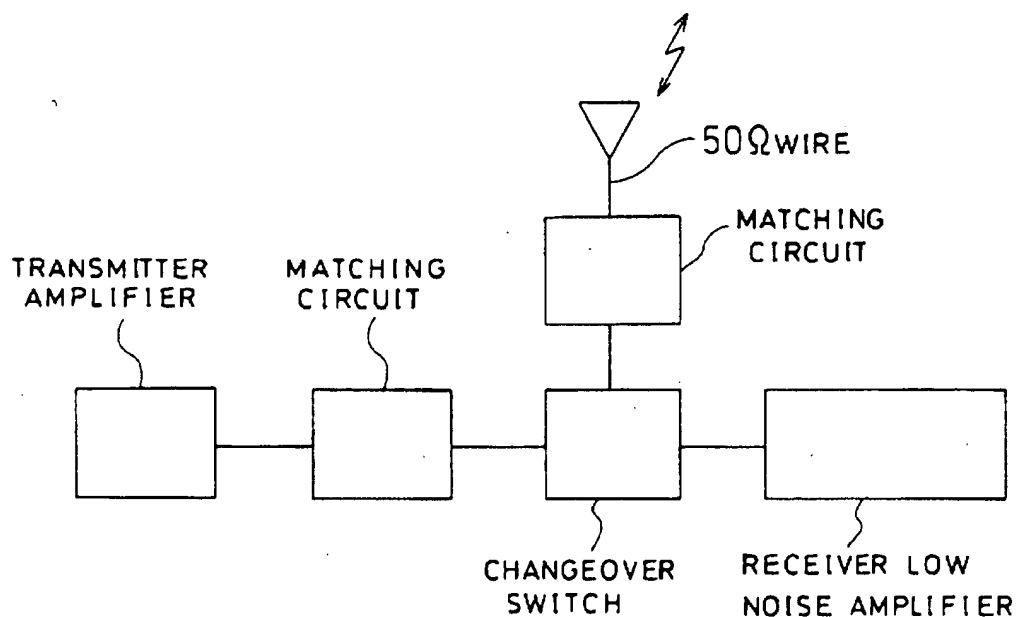


FIG. 5(b)

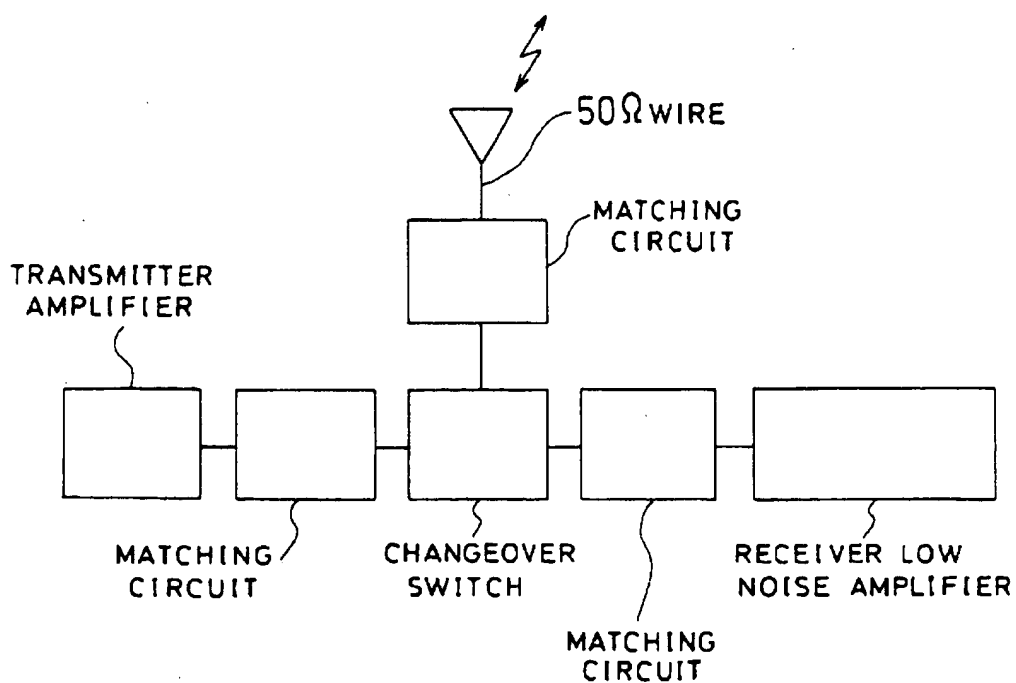


FIG. 6

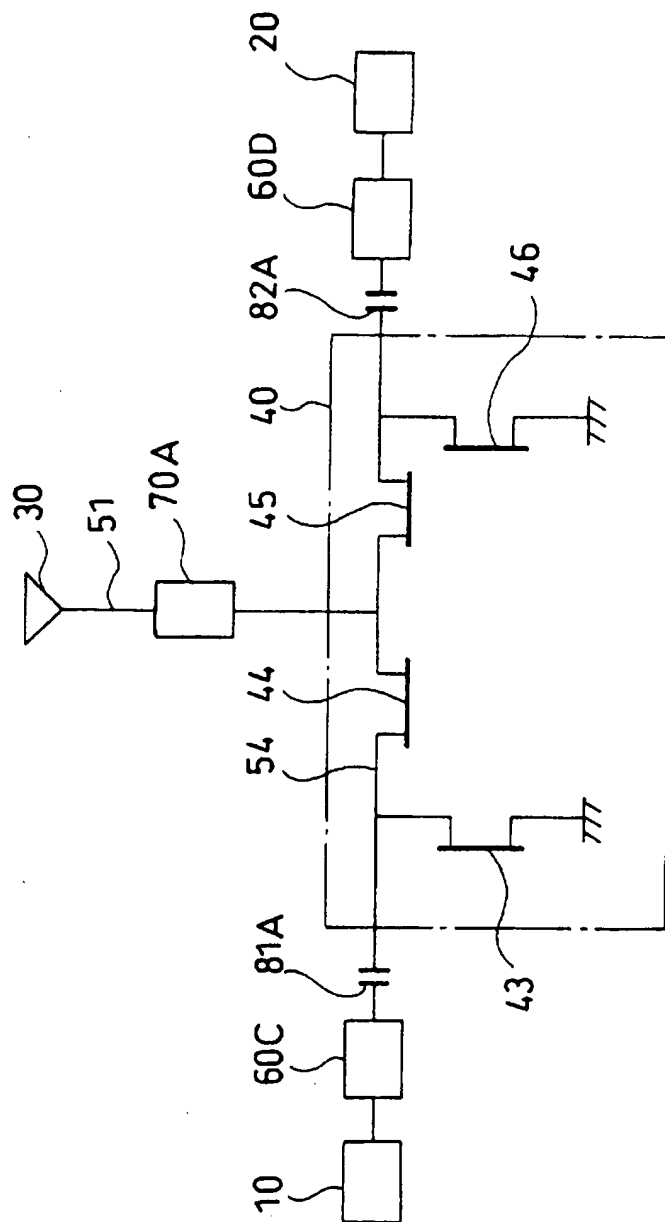


FIG. 7

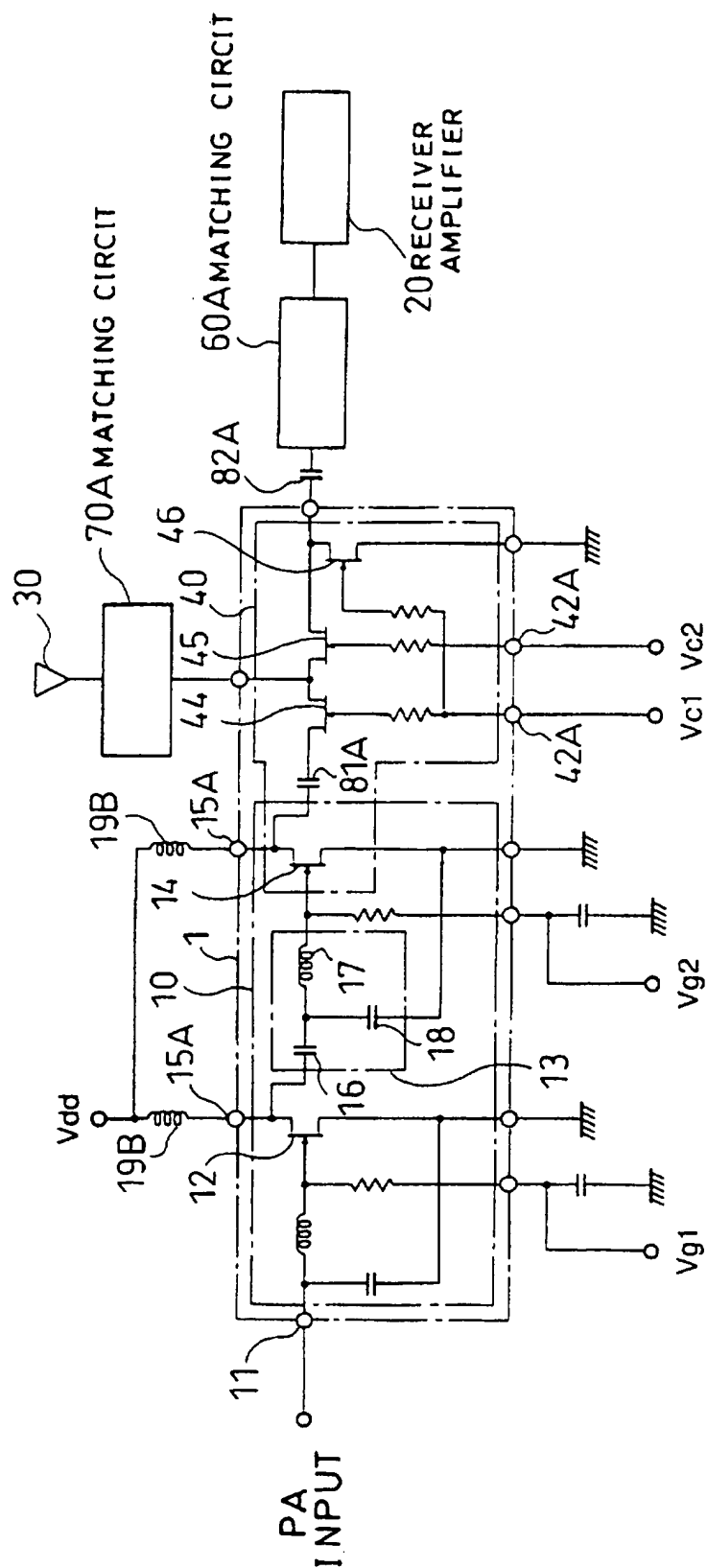
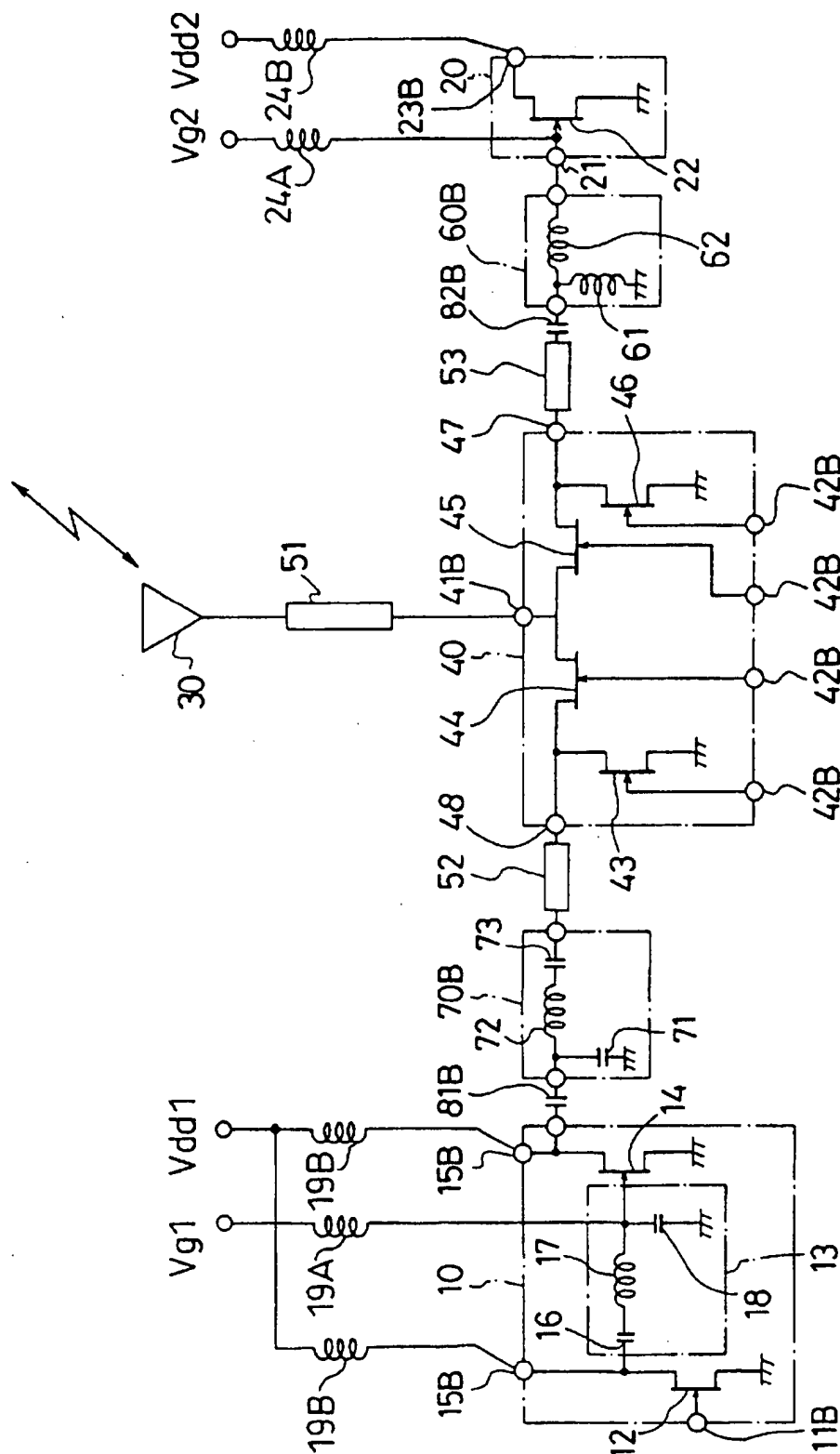


FIG. 8
PRIOR ART



**TRANSMITTING-RECEIVING CIRCUIT FOR
RADIOCOMMUNICATION APPARATUS,
SEMICONDUCTOR INTEGRATED CIRCUIT
DEVICE INCLUDING THE CIRCUIT, AND
RADIOCOMMUNICATION APPARATUS
INCLUDING THE SAME**

BACKGROUND OF THE INVENTION

The present invention relates to a transmitting/receiving circuit suitably used in a radiocommunication apparatus utilizing the same frequency for transmitting and receiving a signal, a semiconductor integrated circuit device including the transmitting/receiving circuit and a radiocommunication apparatus including the same.

Recently, radiocommunication apparatuses such as portable telephones have been developed to be compact, light and inexpensive, and the number of users of such equipment is rapidly increasing. In the conventional communication mode, the transmitting frequency is different from the receiving frequency. Furthermore, attempts have been made to digitalize such radiocommunication apparatuses in order to attain a much larger number of users. In digital radiocommunication apparatuses, transmission and reception can be conducted at the same frequency by transmitting and receiving a signal in a time sharing manner, while two different frequencies are required for each line of the apparatuses of the conventional communication mode.

A transmitter amplifier, a receiver low noise amplifier and a changeover switch for switching between transmission and reception of a transmitting/receiving circuit in a digital radiocommunication apparatus occasionally include gallium arsenide field effect transistors (hereinafter referred to as GaAs FETs) having various properties such as a low voltage operation, high efficiency, a low noise property and a high isolation property.

Furthermore, with the spread of portable wireless apparatuses, there is increasing demand for compact and light equipment. As a result, a large number of attempts have been made to produce a transmitting/receiving circuit including a transmitter power amplifier, a changeover switch, a receiver low noise amplifier, a matching circuit and the like as a semiconductor integrated circuit.

Now, an example of conventional transmitting/receiving circuits will be described referring to an accompanying drawing.

FIG. 8 is a diagram of the configuration of a transmitting/receiving circuit in a conventional digital radiocommunication apparatus using FETs. The transmitting/receiving circuit of FIG. 8 comprises a transmitter amplifier 10, a receiver low noise amplifier 20 and an antenna 30 for transmitting and receiving a signal. A changeover switch 40 switches the connection between the transmitter amplifier 10 and the antenna 30 and the connection between the receiver low noise amplifier 20 and the antenna 30, from one to the other. A first wire 51 having characteristic impedance of 50 Ω connects the antenna 30 to the changeover switch 40. A second wire 52 having characteristic impedance of 50 Ω connects the transmitter amplifier 10 to the changeover switch 40. A third wire 53 having characteristic impedance of 50 Ω connects the receiver low noise amplifier 20 to the changeover switch 40. A receiver matching circuit 60B matches inputs to the receiver low noise amplifier 20, and a transmitter matching circuit 70B matches outputs from the transmitter amplifier 10. A first coupling capacitance 81B couples an alternating current of the output from the transmitter amplifier 10 with an alternating current of the input to

the transmitter matching circuit 70B, and a second coupling capacitance 82B couples an alternating current of the output from the receiver matching circuit 60B with an alternating current of the input to the receiver low noise amplifier 20.

The transmitter amplifier 10 of FIG. 8 comprises an FET 12 at the first stage, another FET 14 at the last stage, power supply terminals 15B, a matching circuit 13, which includes capacitances 16 and 18 and an inductor 17, for matching the front FET 12 with the rear FET 14. An inductor 19A is interposed between the gate terminal of the FET 14 and a bias voltage Vg1, and inductors 19B are interposed between the power supply terminals 15B of the FETs 12 and 14 and a supply voltage Vdd1. An inductor 24A is interposed between the gate terminal of a low noise FET 22 in the receiver low noise amplifier 20 and a bias voltage Vg2, and an inductor 24B is interposed between a reception wave output terminal 23B of the receiver low noise amplifier 20 and a supply voltage Vdd2. The receiver matching circuit 60B includes inductors 61 and 62, and the transmitter matching circuit 70B includes capacitances 71 and 73 and an inductor 72.

This transmitting/receiving circuit is operated as follows:

The receiving operation thereof will be first described.

At the time of receiving a signal, a bias voltage Vg2 is applied to the low noise FET 22 in the receiver low noise amplifier 20 and a supply voltage Vdd2 is applied to the reception wave output terminal 23B, thereby supplying the receiver low noise amplifier 20 with a necessary supply voltage. This amplifies a weak received signal input through the antenna 30. Since there is no need to operate the transmitter amplifier 10 in this case, no voltage is applied thereto for saving the power of a battery.

The received signal having been input through the antenna 30 is transferred through the first wire 51 having characteristic impedance of 50 Ω and supplied to an antenna side input/output terminal 41B of the changeover switch 40. At this point, in the changeover switch 40, a first FET 43 serving as a transmitter shunt FET and a third FET 45 serving as a receiver through FET are supplied with a voltage of, for example, 0 V so as to turn on the FETs 43 and 45, and a second FET 44 serving as a transmitter through FET and a fourth FET 46 serving as a receiver shunt FET are supplied with a voltage of, for example, -5 V so as to turn off the FETs 44 and 46 by a control voltage input through switch control signal input terminals 42B. Therefore, the received signal having been input through the antenna side input/output terminal 41B passes through the third FET 45 in an on state to be transferred to a receiver unit. A transmitter unit is electrically separated from the antenna because the second FET 44 is off, and is short-circuited by the first FET 43 in an on state.

The received signal having passed through the third FET 45 in an on state is transferred from a receiver side terminal 47 of the changeover switch 40 through the third wire 53 having characteristic impedance of 50 Ω and the second coupling capacitance 82B and is input to the receiver matching circuit 60B. The received signal having been input to the receiver matching circuit 60B is subjected to impedance matching by the two inductors 61 and 62 to be input to an input terminal 21 of the receiver low noise amplifier 20. The received signal having been input to the receiver low noise amplifier 20 is amplified by the low noise FET 22 and then output through the reception wave output terminal 23B.

Next, the transmitting operation of the transmitting/receiving circuit will be described.

At the time of transmitting a signal, a supply voltage Vdd1 is applied to the FET 12 at the first stage and the FET 14 at

the last stage of the transmitter amplifier 10, and a bias voltage V_{g1} is applied to the FET 14, thereby power amplifying a modulated signal input to the transmitter amplifier 10 up to a sufficiently high level to be supplied to the antenna 30. Since there is no need to operate the receiver low noise amplifier 20 in this case, no voltage is applied thereto for saving the power of the battery.

The modulated transmission signal is input through a transmission wave input terminal 11B, subjected to first power amplification by the front FET 12, input to the rear FET 14 via the matching circuit 13, and subjected to second power amplification by the FET 14 up to a desired power level. The amplified transmission signal is input to the transmitter matching circuit 70B via the first coupling capacitance 81B, converted to have impedance of $50\ \Omega$ by the transmitter matching circuit 70B and then input to a transmitter side terminal 48 of the changeover switch 40 via the second wire 52 having characteristic impedance of $50\ \Omega$. At this point, in the changeover switch 40, the second FET 44 and the fourth FET 46 are supplied with a voltage of, for example, 0 V so as to be turned on and the first FET 43 and the third FET 45 are supplied with a voltage of, for example, -5 V so as to be turned off by a control voltage input through the switch control signal input terminals 42B. The transmission signal having been input through the transmitter side terminal 48 passes through the second FET 44 in an on state to be transferred toward the antenna 30. The transmission signal having been transferred toward the antenna 30 passes through the first wire 51 having characteristic impedance of $50\ \Omega$, input to the antenna 30, and then output through the antenna 30 as an electric wave.

In the conventional transmitting/receiving circuit, the transmitter amplifier 10 and the receiver low noise amplifier 20 are connected to the changeover switch 40 via the second and third wires 52 and 53 each having characteristic impedance of $50\ \Omega$, respectively. Therefore, a transmission signal output by the transmitter amplifier 10 and a received signal input to the receiver low noise amplifier 20 should be converted to have impedance of $50\ \Omega$. Accordingly, when the transmitter amplifier 10, the receiver low noise amplifier 20 and the changeover switch 40 are desired to be integrated on one chip, the transmitter matching circuit 60B and the receiver matching circuit 70B are also required to be mounted on the same chip, resulting in largely increasing an area occupied by passive devices to be integrated such as inductors. As a result, the chip area is substantially increased, which disadvantageously makes it difficult to decrease the size and the cost of a radiocommunication apparatus. Thus, it is desired to provide a transmitting/receiving circuit realizing a compact and inexpensive radiocommunication apparatus applicable to the new communication mode and a semiconductor integrated circuit device mounting the transmitting/receiving circuit.

In addition, when a signal is switched by the changeover switch 40 at low impedance, the voltage can be decreased and isolation between the transmitter unit and the receiver unit can be improved. However, in the conventional circuit, a signal is switched at impedance of $50\ \Omega$ as described above, and hence, the isolation characteristic is poor. This causes another problem that an FET with a satisfactory isolation characteristic is required to be used. The isolation herein indicates a ratio between signals correctly transferred from the transmitter amplifier 10 to the antenna 30 and signals incorrectly transferred from the transmitter amplifier 10 to the receiver low noise amplifier 20 when the changeover switch 40 is in a state for outputting a transmission signal from the transmitter amplifier 10 to the antenna

30. Having a satisfactory isolation characteristic means few signals are transferred from the transmitter amplifier 10 to the receiver low noise amplifier 20. Actually, there always exist some signals leaked from the transmitter amplifier 10 to the receiver low noise amplifier 20.

SUMMARY OF THE INVENTION

The present invention was devised to solve the aforementioned problems at a stroke so as to make compact a radiocommunication apparatus and improve the isolation characteristic between a transmitter unit and a receiver unit.

A first transmitting/receiving circuit for a radiocommunication apparatus of the invention comprises a transmitter amplifier for amplifying an input transmission signal and outputting the amplified transmission signal; a receiver amplifier for amplifying an input received signal and outputting the amplified received signal; a changeover switch having an antenna side input/output terminal through which the transmission signal is output to an antenna via a wire having prescribed characteristic impedance and the received signal is input from the antenna via the wire, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier via no matching circuit to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier; a receiver matching circuit interposed between the changeover switch and the receiver amplifier for matching the input impedance of the receiver amplifier with the output impedance of the transmitter amplifier; and an antenna side matching circuit interposed between the wire and the changeover switch for matching the characteristic impedance of the wire with the output impedance of the transmitter amplifier.

In the first transmitting/receiving circuit, the transmission signal output from the transmitter amplifier is input to the changeover switch via no matching circuit, while the received signal output from the changeover switch is input to the receiver amplifier via the receiver matching circuit. Therefore, within the changeover switch, the output impedance of the transmitter amplifier is matched with the input impedance of the receiver amplifier, and both the output impedance and the input impedance are small in the changeover switch. As a result, the isolation characteristic of the changeover switch can be improved and the area occupied by the changeover switch can be minimized.

Furthermore, since the characteristic impedance of the wire is matched with the output impedance of the transmitter amplifier by the antenna side matching circuit, the receiver matching circuit has a function to merely match the input impedance of the receiver amplifier with the output impedance of the transmitter amplifier. This results in minimizing the area occupied by the receiver matching circuit. Thus, the size of a chip including the transmitter amplifier, the receiver amplifier and the changeover switch, and in its turn, the size of the radiocommunication apparatus including the chip can be minimized, and the production cost can be decreased.

Since the antenna side matching circuit is interposed between the wire and the changeover switch, when the transmitter amplifier, the receiver amplifier and the changeover switch are integrated on one chip, the antenna side matching circuit can be disposed outside of the chip. This results in a further more compact chip, a further more compact radiocommunication apparatus, and a further lower production cost.

It is preferable that the first transmitting/receiving circuit further comprises a first coupling capacitance interposed

between the transmitter amplifier and the changeover switch and a second coupling capacitance interposed between the changeover switch and the receiver matching circuit.

By adopting this configuration, the coupling state between the transmitter amplifier and the changeover switch can be stabilized, and the coupling state between the changeover switch and the receiver matching circuit can be also stabilized.

In the first transmitting/receiving circuit, the antenna side matching circuit can be directly connected to the antenna side input/output terminal. In this case, the antenna side matching circuit can be formed on the same chip mounting the transmitter amplifier, the receiver amplifier and the changeover switch. Therefore, a still more compact radio-communication apparatus can be realized.

In the first transmitting/receiving circuit, the changeover switch preferably has a transmitter through FET and a transmitter shunt FET connected in series to each other and a receiver through FET and a receiver shunt FET connected in series to each other. The transmitter amplifier preferably has at least one amplifier FET for amplifying the input transmission signal, and the amplifier FET at the last stage of the transmitter amplifier preferably works also as the transmitter shunt FET of the changeover switch.

By adopting this configuration, there is no need to provide a separate transmitter shunt FET in the changeover switch, thereby simplifying the configuration of the transmitting/receiving circuit for a radiocommunication apparatus. Therefore, since the number of required elements can be reduced, the radiocommunication apparatus can be made more compact and can attain higher reliability.

A second transmitting/receiving circuit for a radiocommunication apparatus of the invention comprises a transmitter amplifier for amplifying an input transmission signal and outputting the amplified transmission signal; a receiver amplifier for amplifying an input received signal and outputting the amplified received signal; a changeover switch having an antenna side input/output terminal through which the transmission signal is output to an antenna via a wire having prescribed characteristic impedance and the received signal is input from the antenna via the wire, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier via no matching circuit, from one to the other; a transmitter matching circuit interposed between the transmitter amplifier and the changeover switch for matching the output impedance of the transmitter amplifier with the input impedance of the receiver amplifier; and an antenna side matching circuit interposed between the wire and the changeover switch for matching the characteristic impedance of the wire with the input impedance of the receiver amplifier.

In the second transmitting/receiving circuit, the transmission signal output from the transmitter amplifier is input to the changeover switch via the transmitter matching circuit, while the received signal output by the changeover switch is input to the receiver amplifier via no matching circuit. Therefore, within the changeover switch, the output impedance of the transmitter amplifier is matched with the input impedance of the receiver amplifier, and both the output impedance and the input impedance are small in the changeover switch. As a result, the isolation characteristic of the changeover switch can be improved and the area occupied by the changeover switch can be minimized.

Furthermore, since the characteristic impedance of the wire is matched with the input impedance of the receiver amplifier by the antenna side matching circuit, the transmitter matching circuit has a function merely to match the output impedance of the transmitter amplifier with the input impedance of the receiver amplifier. Therefore, the area occupied by the transmitter matching circuit can be minimized. Thus, a chip including the transmitter amplifier, the receiver amplifier and the changeover switch, and in its turn, the radiocommunication apparatus including the chip can be made compact and the production cost can be reduced.

Since the antenna side matching circuit is interposed between the wire and the changeover switch, when the transmitter amplifier, the receiver amplifier and the changeover switch are integrated on one chip, the antenna side matching circuit can be formed outside of the chip. This results in a further more compact chip, a further more compact radiocommunication apparatus, and a further lower production cost.

A third transmitting/receiving circuit for a radiocommunication apparatus of the invention comprises a transmitter amplifier for amplifying an input transmission signal and outputting the amplified transmission signal; a receiver amplifier for amplifying an input received signal and outputting the amplified received signal; a changeover switch having an antenna side input/output terminal through which the transmission signal is output to an antenna via a wire having prescribed characteristic impedance and the received signal is input from the antenna via the wire, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier, from one to the other; a transmitter matching circuit interposed between the transmitter amplifier and the changeover switch for matching the output impedance of the transmitter amplifier with optimal characteristic impedance of the changeover switch; a receiver matching circuit interposed between the changeover switch and the receiver amplifier for matching the input impedance of the receiver amplifier with the optimal characteristic impedance of the changeover switch; and an antenna side matching circuit interposed between the wire and the changeover switch for matching the characteristic impedance of the wire with the optimal characteristic impedance of the changeover switch.

In the third transmitting/receiving circuit, the transmission signal output from the transmitter amplifier is input to the changeover switch via the transmitter matching circuit, while the received signal output from the changeover switch is input to the receiver amplifier via the receiver matching circuit. Therefore, within the changeover switch, the output impedance of the transmitter amplifier is matched with the input impedance of the receiver amplifier, and both the output impedance and the input impedance are small in the changeover switch. This results in improving the isolation characteristic of the changeover switch.

Since the characteristic impedance of the changeover switch can be optimized, the area occupied by the changeover switch and the insertion loss of a through FET therein can be minimized.

The transmitter matching circuit has a function to merely match the output impedance of the transmitter amplifier with the optimal characteristic impedance of the changeover switch, and the receiver matching circuit has a function merely to match the input impedance of the receiver ampli-

fier with the optimal characteristic impedance of the changeover switch. Accordingly, the areas occupied by the transmitter matching circuit and the receiver matching circuit can be both minimized. Thus, a chip including the transmitter amplifier, the receiver amplifier and the changeover switch, and in its turn, the radiocommunication apparatus including the chip can be made compact and the production cost can be reduced.

Since the antenna side matching circuit is interposed between the wire and the changeover switch, when the transmitter amplifier, the receiver amplifier and the changeover switch are integrated on one chip, the antenna side matching circuit can be formed outside of the chip. This results in a further more compact chip, a further more compact radiocommunication apparatus, and a further lower production cost.

A fourth transmitting/receiving circuit for a radiocommunication apparatus of the invention comprises a transmitter amplifier having at least one amplifier FET for amplifying an input transmission signal; a receiver amplifier for amplifying an input received signal and outputting the amplified received signal; a changeover switch including an antenna side input/output terminal through which the transmission signal is output to an antenna and the received signal is input from the antenna, a transmitter through FET and a transmitter shunt FET connected in series to each other, and a receiver through FET and a receiver shunt FET connected in series to each other, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier, from one to the other. The amplifier FET at the last stage of the transmitter amplifier also works as the transmitter shunt FET of the changeover switch.

In the fourth transmitting/receiving circuit, since the amplifier FET at the last stage of the transmitter amplifier also works as the transmitter shunt FET of the changeover switch, there is no need to separately provide a transmitter shunt FET of the changeover switch. Therefore, the configuration of the transmitting/receiving circuit for a radiocommunication apparatus can be simplified and the number of required elements can be reduced, and hence, the radiocommunication apparatus can become more compact and more reliable.

A first semiconductor integrated circuit device of the invention comprises a semiconductor substrate; a transmitter amplifier formed on the semiconductor substrate for amplifying an input transmission signal and outputting the amplified transmission signal; a receiver amplifier formed on the semiconductor substrate for amplifying an input received signal and outputting the amplified received signal; a changeover switch formed on the semiconductor substrate and having an antenna side input/output terminal through which the transmission signal is output to an antenna via a wire having prescribed characteristic impedance and an antenna side matching circuit for matching the characteristic impedance of the wire with the output impedance of the transmitter amplifier and the received signal is input from the antenna via the wire and the antenna side matching circuit, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier via no matching circuit to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier, from one to the other; and a receiver matching circuit formed on the semi-

conductor substrate and interposed between the receiver amplifier and the changeover switch for matching the input impedance of the receiver amplifier with the output impedance of the transmitter amplifier.

In the first semiconductor integrated circuit device, the transmitter amplifier, the receiver amplifier, the changeover switch and the receiver matching circuit of the first transmitting/receiving circuit are formed on one semiconductor substrate. Accordingly, the transmitter amplifier, the receiver amplifier, the changeover switch and the receiver matching circuit of the transmitting/receiving circuit can be definitely integrated on one chip.

In the first semiconductor integrated circuit device, the antenna side matching circuit can be formed on the semiconductor substrate. In this case, the transmitter amplifier, the receiver amplifier, the changeover switch, the receiver matching circuit and the antenna side matching circuit can be integrated on one chip.

In the first semiconductor integrated circuit device, the changeover switch preferably has a transmitter through FET and a transmitter shunt FET connected in series to each other and a receiver through FET and a receiver shunt FET connected in series to each other, the transmitter amplifier preferably has at least one amplifier FET for amplifying the input transmission signal, and the amplifier FET at the last stage of the transmitter amplifier preferably works also as the transmitter shunt FET of the changeover switch. When this configuration is adopted, there is no need to separately provide a transmitter shunt FET of the changeover switch.

A second semiconductor integrated circuit device of the invention comprises a semiconductor substrate; a transmitter amplifier formed on the semiconductor substrate and having at least one amplifier FET for amplifying an input transmission signal; a changeover switch formed on the semiconductor substrate and having an antenna side input/output terminal through which the transmission signal is output to an antenna and a received signal is input from the antenna, a transmitter through FET and a transmitter shunt FET connected in series to each other, and a receiver through FET and a receiver shunt FET connected in series to each other, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to a receiver amplifier, from one to the other. The amplifier FET at the last stage of the transmitter amplifier also works as the transmitter shunt FET of the changeover switch.

In the second semiconductor integrated circuit device, there is no need to separately provide a transmitter shunt FET of the changeover switch, and hence, the configuration of the transmitting/receiving circuit for a radiocommunication apparatus can be simplified. Therefore, the number of required elements can be reduced, and in addition, there is no need to adjust the transmitting/receiving circuit, which otherwise conventionally requires great efforts. As a result, not only the radiocommunication apparatus can become more compact and more reliable, but also the transmitter amplifier, the receiver amplifier, the changeover switch and the receiver matching circuit can be definitely integrated on one chip with ease.

A first radiocommunication apparatus of the invention comprises an antenna; a wire connected to the antenna and having prescribed characteristic impedance; a transmitter amplifier for amplifying an input transmission signal and outputting the amplified transmission signal; a receiver

amplifier for amplifying an input received signal and outputting the amplified received signal; a changeover switch having an antenna side input/output terminal through which the transmission signal is output to the antenna via the wire and the received signal is input from the antenna via the wire, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier via no matching circuit to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier, from one to the other; a receiver matching circuit interposed between the receiver amplifier and the changeover switch for matching the input impedance of the receiver amplifier with the output impedance of the transmitter amplifier; and an antenna side matching circuit interposed between the wire and the changeover switch for matching the characteristic impedance of the wire with the input impedance of the transmitter amplifier.

A second radiocommunication apparatus of the invention comprises an antenna; a wire connected to the antenna and having prescribed characteristic impedance, a transmitter amplifier for amplifying an input transmission signal and outputting the amplified transmission signal; a receiver amplifier for amplifying an input received signal and outputting the amplified received signal; a changeover switch having an antenna side input/output terminal through which the transmission signal is output to the antenna via the wire and the received signal is input from the antenna via the wire, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier via no matching circuit, from one to the other; a transmitter matching circuit interposed between the transmitter amplifier and the changeover switch for matching the output impedance of the transmitter amplifier with the input impedance of the receiver amplifier; and an antenna side matching circuit interposed between the wire and the changeover switch for matching the characteristic impedance of the wire with the input impedance of the receiver amplifier.

A third radiocommunication apparatus of the invention comprises an antenna; a wire connected to the antenna and having prescribed characteristic impedance; a transmitter amplifier for amplifying an input transmission signal and outputting the amplified transmission signal; a receiver amplifier for amplifying an input received signal and outputting the amplified received signal; a changeover switch having an antenna side input/output terminal through which the transmission signal is output to the antenna via the wire and the received signal is input from the antenna via the wire, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier; a transmitter matching circuit interposed between the transmitter amplifier and the changeover switch for matching the output impedance of the transmitter amplifier with optimal characteristic impedance of the changeover switch; a receiver matching circuit interposed between the changeover switch and the receiver amplifier for matching the input impedance of the receiver amplifier with the optimal characteristic impedance of the changeover switch; and an antenna side matching circuit interposed between the

wire and the changeover switch for matching the characteristic impedance of the wire with the optimal characteristic impedance of the changeover switch.

Any of the first through third radiocommunication apparatuses can attain a reduced size and a lower production cost, and the isolation characteristic of the changeover switch can also be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1a is a schematic diagram of the rough configuration of a conventional transmitting/receiving circuit for a radiocommunication apparatus, and FIG. 1b is a schematic diagram of the rough configuration of a transmitting/receiving circuit for a radiocommunication apparatus according to a first embodiment of the invention;

FIG. 2 is a diagram showing a specific configuration of the transmitting/receiving circuit for a radiocommunication apparatus according to the first embodiment;

FIG. 3 is a Smith chart of an impedance matching state used for describing the operation of the transmitting/receiving circuit for a radiocommunication apparatus of the first embodiment;

FIG. 4 is a schematic diagram of the rough configuration of a transmitting/receiving circuit for a radiocommunication apparatus according to a second embodiment of the invention;

FIG. 5a and 5b are schematic diagrams of the rough configurations of transmitting/receiving circuits for a radiocommunication apparatus according to third and fourth embodiments of the invention, respectively;

FIG. 6 illustrates optimal characteristic impedance of a changeover switch used in the transmitting/receiving circuit for a radiocommunication apparatus of the fourth embodiment;

FIG. 7 is a diagram showing a specific configuration of a transmitting/receiving circuit for a radiocommunication apparatus according to a fifth embodiment of the invention; and

FIG. 8 is a diagram showing a specific configuration of a conventional transmitting/receiving circuit for a radiocommunication apparatus.

DETAILED DESCRIPTION OF THE INVENTION

The present invention will now be described by way of example referring to the accompanying drawings.

(Embodiment 1)

FIG. 1a is a schematic diagram of the rough configuration of a conventional transmitting/receiving circuit for a radiocommunication apparatus and FIG. 1b is a schematic diagram of the rough configuration of a transmitting/receiving circuit for a radiocommunication apparatus of this embodiment.

In the transmitting/receiving circuit of FIG. 1a, as is described above regarding the background art, wires each having characteristic impedance of 50 Ω are respectively provided between an antenna and a changeover switch, between a transmitter amplifier and the changeover switch, and between a receiver low noise amplifier and the changeover switch. Therefore, matching circuits are interposed between the transmitter amplifier and the wire with characteristic impedance of 50 Ω and between the receiver low noise amplifier and the wire with characteristic impedance of 50 Ω .

In contrast, in the transmitting/receiving circuit of FIG. 1b, although an antenna and a changeover switch are connected to each other via a wire having characteristic impedance of $50\ \Omega$, a wire with characteristic impedance of $50\ \Omega$ is interposed neither between a transmitter amplifier and the changeover switch nor between a receiver low noise amplifier and the changeover switch. Furthermore, although a receiver matching circuit is interposed between the receiver low noise amplifier and the changeover switch, there provided no matching circuit between the transmitter amplifier and the changeover switch. In the circuit of FIG. 1b, the impedance is matched between the transmitter amplifier and the wire with characteristic impedance of $50\ \Omega$ by an antenna side matching circuit disposed between the wire with characteristic impedance of $50\ \Omega$ and the changeover switch, and the receiver matching circuit matches the impedance of the transmitter amplifier with that of the receiver low noise amplifier.

Now, a specific configuration of the transmitting/receiving circuit for a radiocommunication apparatus of this embodiment will be described referring to FIG. 2.

The transmitting/receiving circuit of FIG. 2 comprises a transmitter amplifier 10, a receiver low noise amplifier 20, an antenna 30 for transmitting and receiving a signal, and a changeover switch 40 for switching the connection between the transmitter amplifier 10 and the antenna 30 and the connection between the receiver low noise amplifier 20 and the antenna 30, from one to the other. A first wire 51 having characteristic impedance of $50\ \Omega$ is interposed between the antenna 30 and the changeover switch 40. A receiver matching circuit 60A matches the input impedance of the receiver low noise amplifier 20 with the output impedance of the transmitter amplifier 10. An antenna side matching circuit 70A matches the input impedance of the receiver low noise amplifier 20, which is matched with the output impedance of the transmitter amplifier 10 by the receiver matching circuit 60A, with the characteristic impedance $50\ \Omega$ of the first wire 51. A first coupling capacitance 81A directly couples the output of the transmitter amplifier 10 and the input of the changeover switch 40. A second coupling capacitance 82A directly couples the receiver matching circuit 60A and the changeover switch 40. In the circuit of FIG. 2, a matching circuit 13 matches an FET 12 at the first stage with an FET 14 at the last stage, which is not related to the spirit of the invention.

The transmitter amplifier 10, the receiver low noise amplifier 20, the changeover switch 40 and the receiver matching circuit 60A are formed on one semiconductor substrate as an integrated circuit 1.

The transmitter amplifier 10 of FIG. 2 has the FET 12 at the first stage, the FET 14 at the last stage, and the matching circuit 13 including capacitances 16 and 18 and an inductor 17 for matching the FET 12 with the FET 14. The transmitting/receiving integrated circuit 1 is provided with supply terminals 15A. An inductor 19A is interposed between the gate terminal of the rear FET 14 and a bias voltage V_{g1} , and inductors 19B are interposed between the supply terminals 15A and a supply voltage V_{dd1} . The transmitting/receiving integrated circuit 1 is further provided with a reception wave output terminal 23A. An inductor 24A is interposed between the gate terminal of a low noise FET 22 in the receiver low noise amplifier 20 and a bias voltage V_{g2} , and an inductor 24B is interposed between the reception wave output terminal 23A and a supply voltage V_{dd2} . The antenna side matching circuit 70A has capacitances 71 and 73 and an inductor 72.

The operation of this transmitting/receiving circuit for a radiocommunication apparatus will be described referring to FIGS. 2 and 3.

FIG. 3 is a Smith chart showing the output matching state of the transmitter amplifier 10 and the input matching state of the receiver low noise amplifier 20. The input impedance of the receiver low noise amplifier 20 using a GaAs FET is generally positioned around a point A in FIG. 3, and the output impedance of the transmitter amplifier 10 is generally positioned around a point B, $(17-j\ 8.8)\ \Omega$.

In the conventional transmitting/receiving circuit, the input impedance to the receiver low noise amplifier 20 is matched with the impedance of $50\ \Omega$ by the receiver matching circuit 60B and the output impedance of the transmitter amplifier 10 is matched with the impedance of $50\ \Omega$ by the transmitter matching circuit 70B, as described referring to FIG. 8. Specifically, the input impedance of the receiver low noise amplifier 20 at the point A is matched to be positioned at a point C by the receiver matching circuit 60B, and the output impedance of the transmitter amplifier 10 at the point B is matched to be positioned at the point C by the transmitter matching circuit 70B. This is because the input impedance of the receiver low noise amplifier 20 and the output impedance of the transmitter amplifier 10 should be matched with the impedance of the wires having characteristic impedance of $50\ \Omega$.

In this embodiment, in contrast, the input impedance of the receiver low noise amplifier 20 is matched with the output impedance (at the point B) of the transmitter amplifier 10 by the receiver matching circuit 60A. The resistance at the point B is $(17-j\ 8.8)\ \Omega$, which is significantly smaller than the characteristic impedance $50\ \Omega$ of the first wire 51.

The output impedance of the transmitter amplifier 10 and the input impedance of the receiver low noise amplifier 20 both at the point B are matched with the characteristic impedance ($50\ \Omega$) of the first wire 51 by the antenna side matching circuit 70A. In other words, an arrow from the point A to the point B indicates the matching by the receiver matching circuit 60A, and an arrow from the point B to the point C ($50\ \Omega$) indicates the matching by the antenna side matching circuit 70A. The spirit of Embodiment 1 is in that both the input impedance of the receiver low noise amplifier 20 matched to be positioned at the point B and the output impedance of the transmitter amplifier 10 at the point B are matched to be positioned at the point C by the antenna side matching circuit 70A.

Now, the receiving operation of the transmitting/receiving circuit will be described.

A received signal input through the antenna 30 passes through the first wire 51 having characteristic impedance of $50\ \Omega$, subjected to impedance conversion by the antenna side matching circuit 70A, and input to an antenna side input/output terminal 41A. At this point, in the changeover switch 40, a first FET 43 serving as a transmitter shunt FET and a third FET 45 serving as a receiver through FET are on and a second FET 44 serving as a transmitter through FET and a fourth FET 46 serving as a receiver shunt FET are turned off by control signals input through switch control signal input terminals 42A, as is described referring to the conventional circuit. Therefore, the received signal input through the antenna side input/output terminal 41A passes through the third FET 45 in an on state to be transferred to the receiver unit. Further, the transmitter unit is electrically separated from the antenna because the second FET 44 is off, and is short-circuited by the first FET 43 in an on state.

The received signal having passed through the third FET 45 in an on state is input to the receiver matching circuit 60A through the second coupling capacitance 82A. The received signal having been input to the receiver matching circuit

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60A is subjected to the impedance matching by two inductors 61 and 62, amplified by the low noise FET 22 in the receiver low noise amplifier 20, and then output through the reception wave output terminal 23A.

The transmitting operation of this circuit will now be described.

A modulated transmission wave is input to a transmission wave input terminal 11A. The input transmission wave is subjected to first power amplification by the FET 12 at the first stage, input through the matching circuit 13 to the FET 14 at the last stage, and subjected to second power amplification by the FET 14 up to a desired power level. The amplified transmission signal is directly input to the second FET 44 of the changeover switch 40 through the first coupling capacitance 81A. At this point, the changeover switch 40 performs a reverse operation to that in receiving a signal. Specifically, by control signals input through the switch control signal input terminals 42A, the second FET 44 and the fourth FET 46 are turned on and the first FET 43 and the third FET 45 are turned off. Therefore, the transmission signal having been input through the first coupling capacitance 81A passes through the second FET 44 in an on state to be transferred toward the antenna 30. At this point, the receiver unit is electrically separated from the transmitter unit because the third FET 45 is off, and is short-circuited by the fourth FET 46 in an on state. The transmission signal transferred toward the antenna 30 is input to the antenna side matching circuit 70A, subjected to impedance conversion to have characteristic impedance of 50 Ω by the antenna side matching circuit 70A, and input to the antenna 30 through the first wire 51. Then, the transmission signal is output through the antenna 30 as an electric wave.

In Embodiment 1, the input impedance of the receiver low noise amplifier 20 is matched with the output impedance of the transmitter amplifier 10 by the receiver matching circuit 60A in this manner. As a result, there is no need to provide a matching circuit between the transmitter amplifier 10 and the changeover switch 40, and the transmitter amplifier 10 can be directly connected to the changeover switch 40. Thus, it is possible to decrease the characteristic impedance of the changeover switch 40 to be lower than 50 Ω . This results in lowering the characteristic impedance of a portion between the changeover switch 40 and the antenna side matching circuit 70A to be smaller than 50 Ω . Therefore, fewer signals leak from the transmitter amplifier 10 to the receiver low noise amplifier 20 when the changeover switch 40 switches on the connection between the transmitter amplifier 10 and the antenna 30, thereby improving the isolation characteristic. Also, when the changeover switch 40 switches on the connection between the receiver low noise amplifier 20 and the antenna 30, fewer signals leak from the receiver low noise amplifier 20 to the transmitter amplifier 10.

In addition, since the antenna side matching circuit 70A can be disposed between the antenna 30 and the antenna side input/output terminal 41A, the antenna side matching circuit 70A can be taken out of the transmitting/receiving integrated circuit 1. Accordingly, the area of the integrated chip can be decreased, resulting in reducing the size and the cost of the transmitting/receiving circuit.

Furthermore, since the antenna side matching circuit 70A is commonly used in receiving and transmitting a signal, the size of the receiver matching circuit 60A can be decreased, resulting in further reducing the size and the production cost of the entire chip.

In the transmitting/receiving circuit of Embodiment 1, it is possible to integrate the antenna side matching circuit 70A with the transmitting/receiving integrated circuit 1.

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(Embodiment 2)

A semiconductor integrated circuit device of Embodiment 2 of the invention will now be described referring to the accompanying drawing. The semiconductor integrated circuit device of this embodiment realizes the transmitting/receiving circuit for a radiocommunication apparatus of Embodiment 1, and is operated in the same manner as described in Embodiment 1.

FIG. 3 is a diagram showing the layout of the semiconductor integrated circuit device of Embodiment 2, wherein like reference numerals are used to refer to like elements used in Embodiment 1 shown in FIG. 2 and the description thereof is omitted. The FET 12 at the first stage of the transmitter amplifier 10 is constructed with a drain, a gate, a source, a gate and a drain successively illustrated in this order from the left side of the drawing.

The semiconductor integrated circuit device of FIG. 3 comprises a pad 101 for a ground terminal, a pad 102 for the supply terminal 15A, a pad 103 for the antenna side input/output terminal 41A, a pad 104 for the switch control signal input terminal 42A connected to the third FET 45 of the changeover switch 40, a pad 105 for the ground terminal and the source terminal of the FET 12 at the first stage of the transmitter amplifier 10, a pad 106 for the transmission wave input terminal 11A and the gate terminal of the FET 12 at the first stage of the transmitter amplifier 10, a pad 107 for the gate terminal of the second FET 44 of the changeover switch 40, a pad 108 for the switch control signal input terminal 42A connected to the first FET 43 of the changeover switch 40, a pad 109 for the switch control signal input terminal 42A connected to the fourth FET 46 of the changeover switch 40, a pad 110 for the ground terminal, and a pad 111 for the reception wave output terminal 23A.

In this manner, when the entire elements constructing the transmitting/receiving circuit are integrated on one chip, the circuit configuration of Embodiment 1 enables the antenna side matching circuit 70A, which is conventionally required to be integrated in the chip, to be disposed outside of the chip.

In addition, since the antenna side matching circuit 70A is commonly used in transmitting and receiving a signal, the sizes of the inductors 61 and 62 included in the receiver matching circuit 60B can be decreased, resulting in realizing a compact and inexpensive semiconductor integrated circuit device.

The transmitter amplifier 10, the receiver low noise amplifier 20 and the changeover switch 40 of Embodiment 1 use GaAs FETs, which can be replaced with silicon MOSFETs.

(Embodiment 3)

A transmitting/receiving circuit for a radiocommunication apparatus of Embodiment 3 of the invention will now be described referring to the accompanying drawing.

FIG. 5a shows the rough configuration of the transmitting/receiving circuit for a radiocommunication apparatus of this embodiment, which is different from that of Embodiment 1 in the following points: A transmitter matching circuit is provided between a transmitter amplifier and a changeover switch, while no matching circuit is disposed between a receiver low noise amplifier and the changeover switch in this embodiment.

In order to adopt this configuration, a silicon bipolar transistor and a GaAs FET are required to be used in the receiver low noise amplifier and the transmitter amplifier,

respectively. In addition, the input impedance of the silicon bipolar transistor is required to be lower than that of the GaAs FET. In this case, the input impedance of the transmitter amplifier should be lowered by the transmitter matching circuit to be matched with the output impedance of the receiver low noise amplifier.

(Embodiment 4)

A transmitting/receiving circuit for a radiocommunication apparatus of Embodiment 4 of the invention will now be described referring to the accompanying drawings.

FIG. 5b shows the rough configuration of the transmitting/receiving circuit for a radiocommunication apparatus of this embodiment, wherein a transmitter matching circuit is disposed between a transmitter amplifier and a changeover switch and a receiver matching circuit is disposed between a receiver low noise amplifier and the changeover switch. This configuration is apparently similar to that of the conventional transmitting/receiving circuit but is different in the following point: The characteristic impedance of a wire extending between an antenna side matching circuit and an antenna is 50 Ω, while that of a wire extending between the antenna side matching circuit and the changeover switch is set to be optimal for the changeover switch in Embodiment 4.

Thus, in this embodiment, the impedance of the wire from the antenna side matching circuit to the changeover switch is set to be optimal for the changeover switch, and in order to attain the optimal impedance, the transmitter matching circuit is provided between the transmitter amplifier and the changeover switch and the receiver matching circuit is provided between the receiver low noise amplifier and the changeover switch.

Now, the significance of setting the impedance of the portion between the antenna side matching circuit and the changeover switch at an optimal value for the changeover switch will be described referring to FIG. 6.

The configuration of FIG. 6 comprises a transmitter amplifier 10, a receiver low noise amplifier 20, an antenna 30 for transmitting and receiving a signal, a changeover switch 40, a first wire 51 with characteristic impedance of 50 Ω connecting the antenna 30 to the changeover switch 40, a transmitter matching circuit 60C for matching the output impedance of the transmitter amplifier 10 with the optimal characteristic impedance of the changeover switch 40, a receiver matching circuit 60D for matching the input impedance of the receiver low noise amplifier 20 with the optimal characteristic impedance of the changeover switch 40, an antenna side matching circuit for matching the optimal characteristic impedance of the changeover switch 40 with the characteristic impedance of 50 Ω of the first wire 51, a first coupling capacitance 81A for coupling the transmitter matching circuit 60C and the changeover switch 40, and a second coupling capacitance 82A for coupling the receiver low noise amplifier 20 and the changeover switch 40.

First, in the case where the changeover switch 40 switches on the connection between the transmitter amplifier 10 and the antenna 30, insertion loss of the second FET 44 serving as a transmitter through FET will be examined.

When the insertion loss of the second FET 44 is indicated by L, the following expression 1 holds:

$$L = 10 \times \log ((2Z_0 + \text{Ron})/2 \times Z_0)^2 \text{ dB} \quad (1)$$

wherein Z₀ indicates the characteristic impedance of a wire 54 on which the second FET 44 is disposed, and Ron indicates the on resistance of the second FET 44.

In the conventional configuration, since the characteristic impedance Z₀ of the wire 54 is 50 Ω as that of the first wire 51, the following expression holds:

$$L = 10 \times \log ((100 + \text{Ron})/100)^2 \text{ dB}$$

Thus, the insertion loss L depends upon the characteristic (i.e., Ron) of the second FET 44.

In contrast, in the configuration of Embodiment 4, since the transmitter matching circuit BOC is provided, the characteristic impedance of the wire 54 can be set to be optimal for the changeover switch 40. Specifically, by increasing the value of Z₀, the value of $(2Z_0 + \text{Ron})/2 \times Z_0$ can be decreased, thereby minimizing the insertion loss L of the second FET 44.

Furthermore, when the insertion loss L of the second FET 44 is retained to be constant, the gate width of the second FET 44 can be minimized. Specifically, in expression 1, when the on resistance at the time of Z₀=50 Ω is indicated as Ron1, the on resistance at the time of Z₀=100 Ω is indicated as Ron2, and the insertion loss L of the second FET 44 is assumed to be constant, the following expression holds:

$$\begin{aligned} L &= 10 \times \log (2 \times 50 + \text{Ron1})/2 \times 50)^2 \\ &= 10 \times \log (2 \times 100 + \text{Ron2})/2 \times 100)^2 \end{aligned}$$

From this expression, Ron2=2×Ron1 is obtained.

Since the on resistance Ron of an FET is inversely proportional to the gate width W_g of the FET, when the on resistance Ron is doubled, the gate width W_g is halved. Specifically, since the changeover switch 40 occupies the largest area in the transmitting/receiving circuit, the area of the changeover switch 40 can be reduced by optimizing the characteristic impedance of the changeover switch 40 so as to decrease the size of the second FET 44 of the changeover switch 40. Thus, even when the areas of the transmitter and receiver matching circuits 60C and 60D are rather large, the area of the changeover switch 40 can be further decreased, and hence, the entire area of the transmitting/receiving circuit can be made smaller. In this manner, the transmitting/receiving circuit can be made compact.

Furthermore, for the aforementioned reason, when the gate width W_g of the second FET 44 is constant, the insertion loss L of the second FET 44 can be halved.

In this manner, by optimizing the characteristic impedance of the changeover switch 40, the insertion loss of the second FET can be minimized. In addition, by making constant the insertion loss of the second FET, the gate width of the second FET, and in its turn, the area of the second FET can be reduced.

(Embodiment 5)

A transmitting/receiving circuit for a radiocommunication apparatus according to Embodiment 5 of the invention will be described referring to FIG. 7.

The transmitting/receiving circuit of FIG. 7 comprises a transmitter amplifier 10, a receiver low noise amplifier 20, an antenna 30 for transmitting and receiving a signal, a changeover switch for switching the connection between the transmitter amplifier 10 and the antenna 30 and the connection between the receiver low noise amplifier 20 and the antenna 30, from one to the other, a receiver matching circuit 60A for matching the input impedance of the receiver low noise amplifier 20 with the output impedance of the transmitter amplifier 10, an antenna side matching circuit 70A for matching the input impedance of the receiver low noise

amplifier 20 and the output impedance of the transmitter amplifier 10, which are matched with each other by the receiver matching circuit 60A, with characteristic impedance of $50\ \Omega$ of a wire connected to the antenna 30, a first coupling capacitance 81A for directly coupling the output of the transmitter amplifier 10 and the input of the changeover switch 40, and a second coupling capacitance 82A for directly coupling the input of the receiver low noise amplifier 20, which is matched with the output impedance of the transmitter amplifier 10 by the receiver matching circuit 60A, and the output of the changeover switch 40.

The transmitter amplifier 10 and the changeover switch 40 having the above-described configuration are formed on one semiconductor substrate 1.

The transmitting/receiving circuit of Embodiment 5 is characterized in that the changeover switch 40 has an FET 14 disposed at the last stage of the transmitter amplifier 10 and serving as a transmitter shunt FET, a second FET 44 serving as a transmitter through FET, a third FET 45 serving as a receiver through FET, and a fourth FET 46 serving as a receiver shunt FET.

The transmitting operation of this circuit will now be described.

In transmitting a signal, bias voltages V_{g1} and V_{g2} are respectively applied to the gate terminals of an FET 12 at the first stage and the FET 14 at the last stage of the transmitter amplifier 10, and a supply voltage V_{dd} is applied to the source terminals of the FETs 12 and 14, thereby amplifying a modulated signal input to the transmitter amplifier 10 up to a sufficiently high level to be supplied to the antenna 30. In the changeover switch 40, control voltages V_{c1} and V_{c2} are applied to the respective FETs so that those on the transmitter side are turned on and those on the receiver side are turned off. Specifically, for example, the gate terminals of the second FET 44 and the fourth FET 46 are supplied with a voltage of 0 V as the control voltage V_{c1} , and the gate terminal of the third FET 45 is supplied with a voltage of -5 V as the control voltage V_{c2} . In this case, since there is no need to operate the receiver low noise amplifier 20, no supply voltage is applied to the receiver low noise amplifier 20.

The receiving operation of the circuit will now be described.

In receiving a signal, a necessary supply voltage is applied to the receiver low noise amplifier 20, thereby allowing the receiver low noise amplifier 20 to amplify a weak signal that has been input from the antenna 30 through the antenna side matching circuit 70A, the changeover switch 40, the second coupling capacitance 82A and the receiver matching circuit 60A to the receiver low noise amplifier 20. It goes without saying that a high frequency signal input to the receiver low noise amplifier 20 at this point has been subjected to impedance matching by the antenna side matching circuit 70A and the receiver matching circuit 60A as is described referring to Embodiment 1. In the changeover switch 40, the control voltages V_{c1} and V_{c2} and the bias voltage V_{g2} are applied to the respective FETs so that those on the transmitter side are turned off and those on the receiver side are turned on. Specifically, for example, the second FET 44 and the fourth FET 46 are supplied with a voltage of -5 V as the control voltage V_{c1} and the third FET 45 is supplied with a voltage of 0 V as the control voltage V_{c2} .

The FET 14 at the last stage of the transmitter amplifier 10 serving as the transmitter shunt FET is supplied with a voltage of 0 V. In receiving a signal, no supply voltage is applied to the transmitter amplifier 10 in order to save power

of the battery. Therefore, even when the grounded FET 14 at the last stage is on, no drain current flows therethrough. Thus, a high frequency signal can be grounded. In this manner, the FET 14 at the last stage of the transmitter amplifier 10 can work as the transmitter shunt FET of the changeover switch 40. Specifically, in transmitting a signal, since the FET 14 at the last stage of the transmitter amplifier 10 works as an FET at the last stage of the transmitter amplifier 10, the gate terminal thereof is supplied with the bias voltage V_{g2} of, for example, -5 V. In receiving a signal, the FET 14 at the last stage of the transmitter amplifier 10 works as the transmitter shunt FET of the changeover switch 40, and hence, the gate terminal thereof is supplied with the bias voltage V_{g2} of, for example, 0 V.

Thus, this embodiment can simplify the configuration of a transmitting/receiving circuit for a radiocommunication apparatus. In addition, when the transmitting/receiving circuit is formed as a semiconductor integrated circuit, the number of the elements contained therein can be decreased, the size of the resultant radiocommunication apparatus can be minimized, the area of the semiconductor integrated circuit can be also minimized, and there is no need to adjust a high frequency signal. This results in a low production cost of the radiocommunication apparatus.

We claim:

1. A transmitting/receiving circuit for a radiocommunication apparatus comprising:

a transmitter amplifier for amplifying an input transmission signal and outputting the amplified transmission signal;

a receiver amplifier for amplifying an input received signal and outputting the amplified received signal;

a changeover switch having an antenna side input/output terminal through which the transmission signal is output to an antenna via a wire having prescribed characteristic impedance and the received signal is input from the antenna via the wire, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier via no matching circuit to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier, from one to the other;

a receiver matching circuit interposed between the changeover switch and the receiver amplifier for matching input impedance of the receiver amplifier with output impedance of the transmitter amplifier; and an antenna side matching circuit interposed between the wire and the changeover switch for matching the characteristic impedance of the wire with the output impedance of the transmitter amplifier;

wherein the changeover switch has a transmitter through FET and a transmitter shunt FET connected in series to each other and a receiver through FET and a receiver shunt FET connected in series to each other.

the transmitter amplifier has at least one amplifier FET for amplifying the input transmission signal, and the amplifier FET at a last stage of the transmitter amplifier also works as the transmitter shunt FET of the changeover switch.

2. A transmitting/receiving circuit for a radiocommunication apparatus comprising:

a transmitter amplifier for amplifying an input transmission signal and outputting the amplified transmission signal;

- a receiver amplifier for amplifying an input received signal and outputting the amplified received signal;
 - a changeover switch having an antenna side input/output terminal through which the transmission signal is output to an antenna via a wire having prescribed characteristic impedance and the received signal is input from the antenna via the wire, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier, from one to the other;
 - a transmitter matching circuit interposed between the transmitter amplifier and the changeover switch for matching output impedance of the transmitter amplifier with input impedance of the receiver amplifier; and
 - an antenna side matching circuit interposed between the wire and the changeover switch for matching the characteristic impedance of the wire with the input impedance of the receiver amplifier.
3. A transmitting/receiving circuit for a radiocommunication apparatus comprising:
- a transmitter amplifier for amplifying an input transmission signal and outputting the amplified transmission signal;
 - a receiver amplifier for amplifying an input received signal and outputting the amplified received signal;
 - a changeover switch having an antenna side input/output terminal through which the transmission signal is output to an antenna via a wire having prescribed characteristic impedance and the received signal is input from the antenna via the wire, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier, from one to the other;
 - a transmitter matching circuit interposed between the transmitter amplifier and the changeover switch for matching output impedance of the transmitter amplifier with optimal characteristic impedance of the changeover switch;
 - a receiver matching circuit interposed between the changeover switch and the receiver amplifier for matching input impedance of the receiver amplifier with the optimal characteristic impedance of the changeover switch;
 - an antenna side matching circuit interposed between the wire and the changeover switch for matching the characteristic impedance of the wire with the optimal characteristic impedance of the changeover switch.
4. A transmitting/receiving circuit for a radiocommunication apparatus comprising:
- a transmitter amplifier having at least one amplifier FET for amplifying an input transmission signal;
 - a receiver amplifier for amplifying an input received signal and outputting the amplified received signal; and
 - a changeover switch having an antenna input/output terminal through which the transmission signal is output to an antenna and the received signal is input from the antenna, a transmitter through FET and a transmitter shunt FET connected in series to each other, and a receiver through FET and a receiver shunt FET connected in series to each other, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side

- inputted in series to each other, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier, from one to the other.
- wherein the amplifier FET at a last stage of the transmitter amplifier works also as the transmitter shunt FET of the changeover switch.
5. A semiconductor integrated circuit device comprising:
- a semiconductor substrate;
 - a transmitter amplifier formed on the semiconductor substrate for amplifying an input transmission signal and outputting the amplified transmission signal;
 - a receiver amplifier formed on the semiconductor substrate for amplifying an input received signal and outputting the amplified received signal;
 - a changeover switch formed on the semiconductor substrate having an antenna side input/output terminal through which the transmission signal is output to an antenna via a wire having prescribed characteristic impedance and an antenna side matching circuit for matching the characteristic impedance of the wire with output impedance of the transmitter amplifier and the received signal is input from the antenna via the wire and the antenna side matching circuit, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier via no matching circuit to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier, from one to the other; and
 - a receiver matching circuit formed on the semiconductor substrate and interposed between the receiver amplifier and the changeover switch for matching input impedance of the receiver amplifier with the output impedance of the transmitter amplifier;
- wherein the changeover switch has a transmitter through FET and a transmitter shunt FET connected in series to each other and a receiver through FET and a receiver shunt FET connected in series to each other.
- the transmitter amplifier has at least one amplifier FET for amplifying the input transmission signal; and the amplifier FET at a last stage of the transmitter amplifier works also as the transmitter shunt FET of the changeover switch.
6. A semiconductor integrated circuit device comprising:
- a semiconductor substrate;
 - a transmitter amplifier formed on the semiconductor substrate and having at least one amplifier FET for amplifying an input transmission signal; and
 - a changeover switch formed on the semiconductor substrate and having an antenna input/output terminal through which the transmission signal is output to an antenna and a received signal is input from the antenna, a transmitter through FET and a transmitter shunt FET connected in series to each other, a receiver through FET and a receiver shunt FET connected in series to each other, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side

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input/output terminal to the receiver amplifier, from one to the other.

wherein the amplifier FET at a last stage of the transmitter amplifier works also as the transmitter shunt FET of the changeover switch.

7. A radiocommunication apparatus comprising:

an antenna;

a wire connected to the antenna and having prescribed characteristic impedance;

a transmitter amplifier for amplifying an input transmission signal and outputting the amplified transmission signal;

a receiver amplifier for amplifying an input received signal and outputting the amplified received signal;

a changeover switch having an antenna side input/output terminal through which the transmission signal is output to the antenna via the wire and the received signal is input from the antenna via the wire, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier via no matching circuit, from one to the other;

a transmitter matching circuit interposed between the transmitter amplifier and the changeover switch for matching output impedance of the transmitter amplifier with input impedance of the receiver amplifier; and

an antenna side matching circuit interposed between the wire and the changeover switch for matching the characteristic impedance of the wire with the input impedance of the receiver amplifier.

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8. A radiocommunication apparatus comprising:

an antenna;

a wire connected to the antenna and having prescribed characteristic impedance;

a transmitter amplifier for amplifying an input transmission signal and outputting the amplified transmission signal;

a receiver amplifier for amplifying an input received signal and outputting the amplified received signal;

a changeover switch having an antenna side input/output terminal through which the transmission signal is output to the antenna via the wire and the received signal is input from the antenna via the wire, for switching a first connection state for outputting the transmission signal received from the transmitter amplifier to the antenna side input/output terminal and a second connection state for outputting the received signal received through the antenna side input/output terminal to the receiver amplifier, from one to the other;

a transmitter matching circuit interposed between the transmitter amplifier and the changeover switch for matching output impedance of the transmitter amplifier with optimal characteristic impedance of the changeover switch;

a receiver matching circuit interposed between the changeover switch and the receiver amplifier for matching input impedance of the receiver amplifier with the optimal characteristic impedance of the changeover switch; and

an antenna side matching circuit interposed between the wire and the changeover switch for matching the characteristic impedance of the wire with the optimal characteristic impedance of the changeover switch.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,784,687
DATED : July 21, 1998
INVENTOR(S) : Itoh et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page:

In the Foreign Application Priority Data section, change "6-20573" to --6-205073--.

Signed and Sealed this
Twenty-third Day of May, 2000

Attest:



Q. TODD DICKINSON

Attesting Officer

Director of Patents and Trademarks